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# Quasi-Z-Source Inverter Based Bi-Directional DC/DC Converter: Analysis of Experimental Results

J. Zakis<sup>1</sup>, D. Vinnikov<sup>1</sup>, I. Roasto<sup>1</sup>, L. Ribickis<sup>2</sup>

<sup>1</sup> Department of Electrical Drives and Power Electronics, Tallinn University of Technology  
Ehitajate tee 5, 19086 Tallinn (Estonia), Phone:+372 6203709,  
e-mail: janis.zakis@iee.org

<sup>2</sup> Institute of Industrial Electronics and Electrical Engineering, Riga Technical University  
Kronvalda blvd. 1, Riga, LV-1010 (Latvia)  
Phone number:+371 67089415, e-mail: leonids.ribickis@rtu.lv

**Abstract**-This paper presents simulation and experimental results of a quasi-Z-source inverter (qZSI) based bi-directional DC/DC converter for supercapacitor (SC) interfacing. The bi-directional capability provides both the charging and discharging of the SC. During the charging mode the converter operates as a conventional VSI performing the voltage buck function, but during the discharging mode the converter operates as a qZSI based step-up DC/DC converter performing the voltage boost function. The proposed converter discussed was tested in both operating modes - SC charging and discharging. Theoretical assumptions are proved by the PSIM simulation results and verified experimentally on a 500 W laboratory prototype. The most important results obtained are outlined.

## I. INTRODUCTION

Supercapacitor (SC), one of the most promising high power storage element, is widely used in different industrial applications. But one of the most challenging applications of a SC is energy buffering in distributed power generation systems powered by fuel cells (FC) and/or photovoltaic (PV).

Since residential power supply systems with FC and/or PV cannot respond fast at short high power demand spikes, a short term controllable support system with a SC should be introduced. The support system should be connected at the supported system (SS) DC bus. In most cases SS side DC bus voltage ( $U_{SS}$ ) should be 600 V for residential applications, which is enough to modulate 3-phase (400 VAC) or 1-phase (230 VAC) sine wave.

Since SC properties do not allow switching it directly to the SS DC bus, it is necessary to elaborate a suitable power electronic interface which could provide reliable energy transfer between the SC and the SS [1]. Moreover, the interface converter should be able to provide bi-directional power flow in order to charge or discharge the SC.

The aim of this paper is to verify theoretical results obtained by the power electronics group of Tallinn University of Technology in 2009 [2]. For this purpose the novel interface converter model for SC applications was analyzed and tested. The general power circuit of the proposed converter is presented in Fig. 1. It consists of a voltage-source half-bridge inverter (VSI) at the supported energy system side, a medium frequency isolation transformer and a voltage-fed quasi-Z-source inverter (qZSI) on the SC side. In our previous research [2] we used full-bridge VSI on the SS side but now we used the half-bridge VSI in SS side in order to reduce the transformer turns ratio. Also, in the places of the cascaded qZS-network [3]-[6], the single stage qZS-network was used.

In general, the operation modes of the proposed bi-directional converter can be subdivided as the charging mode and the discharging mode of the SC [2].

During the charging of the SC, the converter operates in the voltage buck mode and the charging process of the SC is controlled by the SS side half-bridge VSI. In the energy recovery mode, the supported energy system is being supplied from the SC. To ensure the constant DC-link voltage ( $U_{DC}$ ) level in the conditions of the discharging of the SC the qZSI with the shoot-through PWM control is used to boost the decreasing voltage of the SC [7].

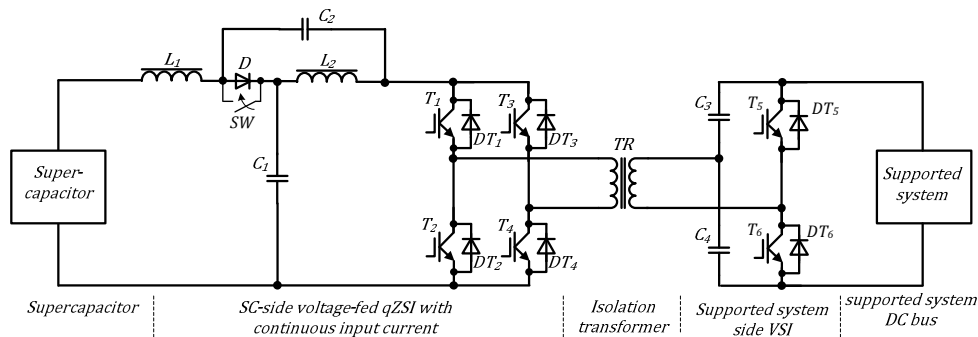


Fig. 1. General power circuit of the proposed bi-directional DC/DC converter for SC interfacing.

## II. OPERATION MODES OF THE PROPOSED CONVERTER

As mentioned above, the proposed interface converter operates in two modes - SC charging and discharging. The operation modes will be described in more detail below.

### A. Charging Mode of the SC

Charging mode of the discussed converter can be realized if the SS DC bus voltage ( $U_{SS}$ ) is at its rated value. If it is so, then the SC is being charged up to its nominal voltage ( $U_{SC}$ ). In other words, we can say that the converter operates in the buck mode performing power transfer from the SS DC-bus to the SC. The general power circuit configuration in the charging mode is shown in Fig. 2.

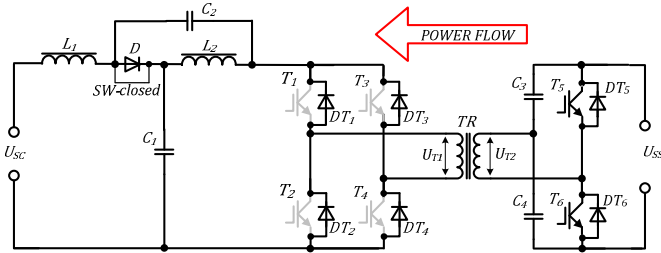


Fig. 2. General power circuit of the interface converter in the charging mode.

In this operation mode the qZSI transistors ( $T_1...T_4$ ) are not conducting, but anti-parallel diodes ( $DT_1...DT_4$ ) operate as full bridge rectifier. The diode  $D$  of the qZS-network is shortened with  $SW$  (contactor) and passive elements ( $L_1$ ,  $L_2$ ,  $C_1$ , and  $C_2$ ) of the qZS-network perform as a low-pass filter.

The SC charging process can be regulated by adjusting the SS side half-bridge VSI transistor ( $T_5$ ,  $T_6$ ) duty cycle  $D$ . Neglecting losses in the circuit elements, the voltage of the SC ( $U_{SC}$ ) during the charging mode is

$$U_{SC} = \frac{D \cdot U_{SS}}{n}, \quad (1)$$

where  $U_{SS}$  is the supported system DC bus voltage,  $D$  is the duty cycle of the VSI switches ( $T_5...T_6$ ) and  $n$  is the turns ratio of the isolation transformer:

$$n = \frac{U_{T2}}{U_{T1}}, \quad (2)$$

where  $U_{T1}$  and  $U_{T2}$  are the amplitude voltages of the primary (SC side) and the secondary (SS side) windings of the isolation transformer, respectively.

### B. Discharging Mode of SC

If the SS DC bus voltage drops during the operation, the proposed interface converter should provide the energy recovery function. It is achieved by the discharging of the SC. The power circuit configuration in the discharging mode is shown in Fig. 3. During the discharging mode, the switch  $SW$  is opened and power flows from the SC to the SS. The power flow is controlled by the qZSI power transistors ( $T_1...T_4$ ). The SS side half-bridge VSI diodes  $DT_5$  and  $DT_6$  of the power

modules ( $T_5$  and  $T_6$ ) together with capacitors  $C_3$  and  $C_4$  act as a voltage doubler rectifier (VDR).

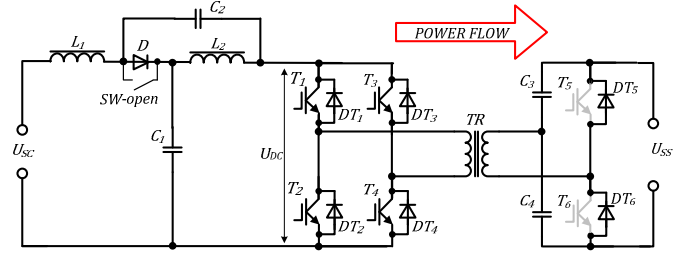


Fig. 3. General power circuit of the interface converter in the discharging mode.

It is well known that during the discharging of the SC its voltage level decreases. To provide the DC-link voltage ( $U_{DC}$ ) in the rated level of the converter the SC voltage ( $U_{SC}$ ) should be preregulated. For that reason we should use the major advantage of the qZSI, i.e. the voltage boost capability by implementing special switching state of qZSI transistors - shoot-through state [7]–[9]. Shoot-through state is simultaneous conduction of both transistors of one inverter leg transistors realized in order to boost the converter input voltage ( $U_{SC}$ ). It should be mentioned that this operating state is forbidden in traditional VSI because of short circuiting of DC capacitors.

While discharging of the SC, the converter must ensure stabilized voltage on the supported system DC-bus ( $U_{SS}$ ) that could be evaluated as

$$U_{SS} = 2 \cdot n \cdot U_{DC}. \quad (3)$$

The proposed converter is intended for operation conditions when the SC voltage ( $U_{SC}$ ) decreases up to half of the nominal ( $0.5U_{SC}$ ). Despite SC voltage decrease, the qZSI should provide voltage preregulation in order to ensure the desired DC-link voltage ( $U_{DC}$ ) level of the interface converter within the whole operating interval. The SC voltage boost can be achieved by changing the shoot-through duty cycle  $D_S$

$$U_{DC} = U_{SC} \frac{1}{1 - 2D_S}, \quad (4)$$

where  $D_S = \frac{t_S}{T}$ ,

where  $t_S$  is the duration of shoot-through and  $T$  is the period.

The maximal shoot-through duty cycle ( $D_{S,max}$ ) should be associated with the minimal SC voltage:

$$D_{S,max} = \frac{1}{2} \cdot \left( 1 - \frac{U_{SC,min}}{U_{DC}} \right). \quad (5)$$

The minimal shoot-through duty cycle ( $D_{S,min}$ ) is associated with the rated operating voltage of the SC:

$$D_{S,min} = \frac{1}{2} \cdot \left( 1 - \frac{U_{SC}}{U_{DC}} \right). \quad (6)$$

### III. SIMULATION RESULTS

To verify the analysis [2] a simulation model was developed in simulation software PSIM. Both operation modes - SC charging and discharging (Figs. 2 and 3) were studied. The parameters of the SC stack of two Maxwell Technologies SC modules (PCM14014) connected in series with a total capacitance value of 85 F, rated voltage 28.8 V and equivalent series resistance 20 mΩ were taken as an example for the simulations. General operating and component ratings for the proposed converter are summarized in Table I.

TABLE I  
GENERAL OPERATION AND COMPONENT RATINGS FOR THE PROPOSED CONVERTER

Parameter	Value
Rated power of converter $P$	500 W
Capacitance of capacitors $C_1, C_2$	730 $\mu$ F
Capacitance of capacitors $C_3, C_4$	220 $\mu$ F
Capacitance of supercapacitor stack $C_{SC}$	70 F
Transformer turns ratio, $n$	1:1
Transformer operation frequency, $f_{TR}$	15 kHz
<i>Charging mode</i>	
Supported system voltage, $U_{SS}$	60 V
SC-voltage, $U_{SC}$	28.8 V
Duty cycle of VSI switches, $D$	0.49
<i>Discharging mode</i>	
Rated SC voltage, $U_{SC}$	28.8 V
Minimal SC voltage, $U_{SC,min}$	14.4 V
Desired DC-link voltage amplitude, $U_l$	30 V
Duty cycle of qZSI switches in active states, $D_A$	0.35
Duty cycle of qZSI switches in shoot-through states, $D_S$	0.02...0.26

#### A. Charging Mode

It was assumed that during the charging mode, the SC is charged up to 28.8 V. The supported system side VSI was operated without dead time at the highest possible duty cycle  $D=0.49$ . SC is never discharged fully empty. It is considered empty when the terminal voltage of the SC has decreased approximately to half of nominal. That is automatically also initial voltage while charging.

Also, wire active resistances and inductances were taken into account. The operation frequency of the isolation transformer during the charging mode was 15 kHz.

Fig. 4 shows the charging process of the SC in the interval of 40 s.

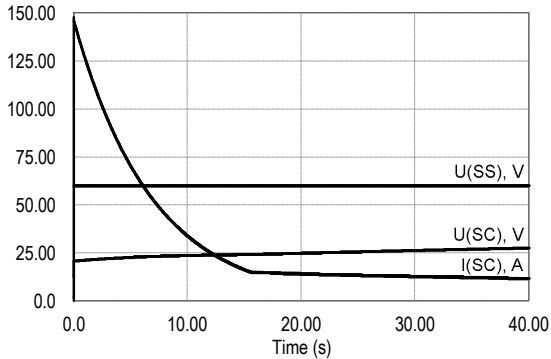


Fig. 4. Operating waveforms of the proposed converter during the SC charging process: SS DC bus voltage ( $U_{SS}$ ), SC stack current ( $I_{SC}$ ) and SC stack voltage ( $U_{SC}$ ).

It can be seen that the SS system DC bus voltage  $U_{SS}$  remains the same, but the SC current  $I_{SC}$  decreases proportionally to the SC voltage  $U_{SC}$  growth.

Fig. 5 shows the voltage waveforms of the SS system DC bus  $U_{SS}$ , transformer  $U_{TR}$ , DC-link voltages  $U_{SS}$  (a) and transformer voltage  $U_{TR}$  and current  $I_{TR}$  (b). Since the half-bridge VSI was used in the SS side, the transformer  $U_{TR}$  and the DC-link voltage  $U_{DC}$  amplitude (30 V) is half of the SS DC bus voltage  $U_{SS}$  amplitude (60 V).

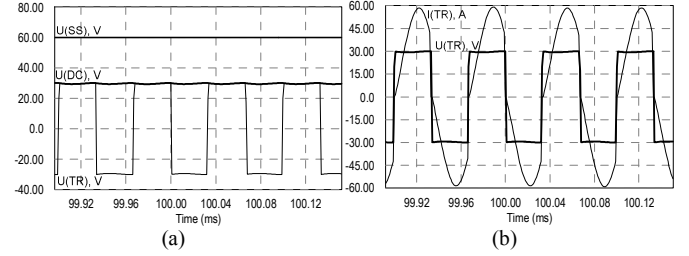


Fig. 5. Simulation results of the proposed converter during the SC charging mode: SS side voltage ( $U_{SS}$ ), transformer voltage ( $U_{TR}$ ), DC-link voltage ( $U_{DC}$ ) (a) and transformer voltage ( $U_{TR}$ ), transformer current ( $I_{TR}$ ) (b).

Finally, Fig. 6 shows that the SC is being charged up to the rated voltage  $U_{SC}$  if the interface converter SS side voltage  $U_{SS}$  is at the predefined value (60 V).

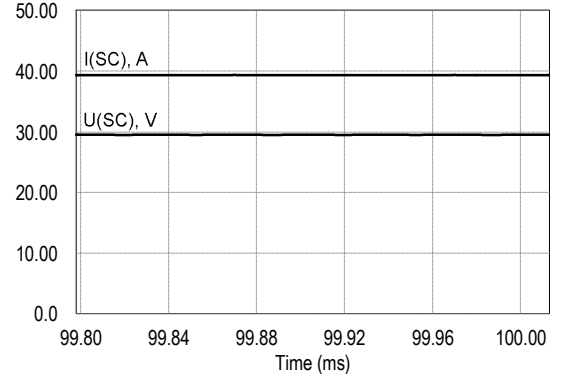


Fig. 6. Simulation results of the proposed converter during the SC charging mode: SC voltage ( $U_{SC}$ ) and SC current ( $I_{SC}$ ).

#### B. Discharging Mode

The circuit configuration in Fig. 3 was used in simulations. The simulations were made at two extremes when the SC voltage  $U_{SC}$  is at its rated value (28.8 V) and at half of the rated value (14.4). It means that in order to provide constant DC-link voltage  $U_{DC}$  also, the minimal shoot-through duty cycle  $D_{S,min}$  and maximal shoot-through duty cycle  $D_{S,max}$  of the qZSI should be introduced.  $U_{SC,max}$  should be associated with  $D_{S,min}=0.02$  and  $U_{SC,min}$  should be associated with  $D_{S,max}=0.26$ . The operation frequency of the isolation transformer during the discharging mode is 15 kHz.

##### Operation with 20 % of full load

First simulations were made with  $U_{SC}=14.4$  V and  $U_{SC}=28.8$  V at a load resistance of 36  $\Omega$  that provides the converter power of 100 W.

Fig. 7 shows two conditions when the SC voltage  $U_{SC}$  is nominal (Fig. 7a) and when the SC voltage is half of the nominal  $0.5U_{SC}$  (Fig. 7b). It is obvious that to provide the constant power rating of the converter the SC current  $I_{SC}$  have to increases (Fig. 7b).

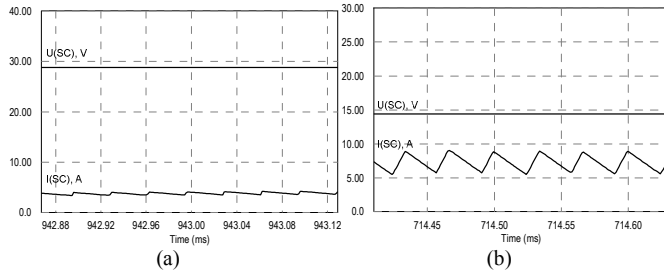


Fig. 7. Simulation results of the proposed converter during the SC discharging mode: SC stack voltage ( $U_{SC}$ ) and current ( $I_{SC}$ ) at nominal (28.8 V) (a) and at half of nominal (14.4 V) (b) voltage.

The nominal SC voltage  $U_{SC}$  and minimal shoot-through duty cycle of the qZSI (0.02) can provide the nominal DC-link  $U_{DC}$ , transformer  $U_{TR}$  and SS side DC bus  $U_{SS}$  voltage amplitudes (Fig. 8a). Despite the operating voltage of the SC  $U_{SS}$  decrease up to half of the nominal  $0.5U_{SC}$  the DC link voltage as well as  $U_{TR}$  and  $U_{SS}$  can be kept on the predefined level by the implementation of the maximal shoot-through duty cycle (0.26) (Fig. 8b).

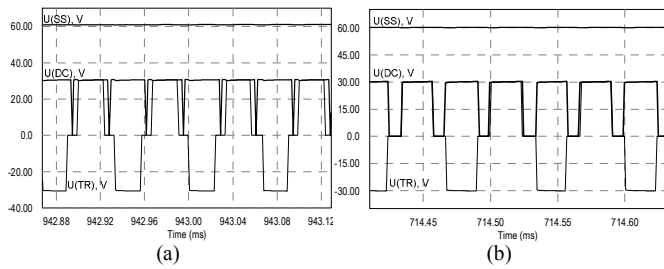


Fig. 8. Simulation results of the proposed converter during the SC discharging mode: DC-link voltage ( $U_{DC}$ ), transformer voltage ( $U_{TR}$ ), SS DC bus voltage ( $U_{SS}$ ), at SC stack nominal (28.8 V) (a) and half of nominal (14.4 V) (b) voltage.

Irrespective of the fact that the SC  $U_{SC}$  voltage can decrease the SS DC bus voltage  $U_{SS}$  and current  $I_{SC}$  are the same in the case of nominal and half of the nominal voltage of the SC (Fig. 9a and b).

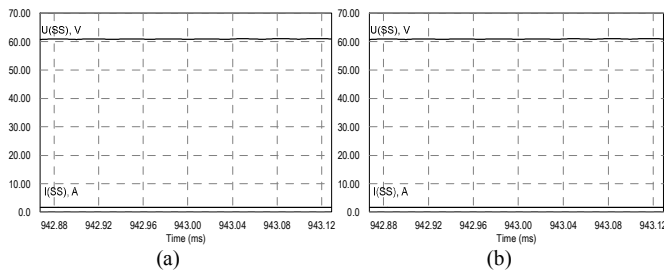


Fig. 9. Simulation results of the proposed converter during the SC discharging mode: SS side voltage ( $U_{SS}$ ) and current ( $I_{SS}$ ) at SC stack nominal (28.8 V) (a) and half of nominal (14.4 V) (b) voltage.

### Operation with a full load

The same converter topology was used for the simulations with a load resistance of  $7.2 \Omega$ , which provides the 500 W load of the proposed converter. Also, in this case two experiments at the nominal ( $U_{SC}=28.8 \text{ V}$ ) and half of the nominal ( $0.5U_{SC}=14.4 \text{ V}$ ) value of the SC voltage were made. Fig. 10 shows that the SC current  $I_{SC}$  is higher at the power rating of 500 W than in the case of 100 W, particularly in the case of higher voltage boost.

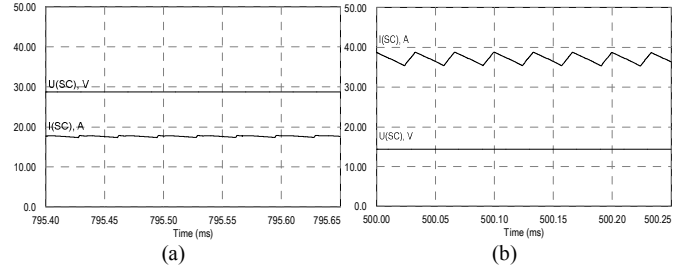


Fig. 10. Simulation results of the proposed converter during the SC discharging mode: SC stack voltage ( $U_{SC}$ ) and current ( $I_{SC}$ ) at nominal (28.8 V) (a) and half of nominal (14.4 V) (b) voltage.

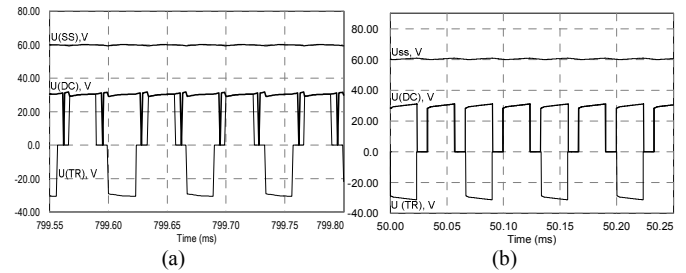


Fig. 11. Simulation results of the proposed converter during the SC discharging mode: DC-link voltage ( $U_{DC}$ ), transformer voltage ( $U_{TR}$ ), SS DC bus voltage ( $U_{SS}$ ), at SC stack nominal (28.8 V) (a) and half of nominal (14.4 V) (b) voltage.

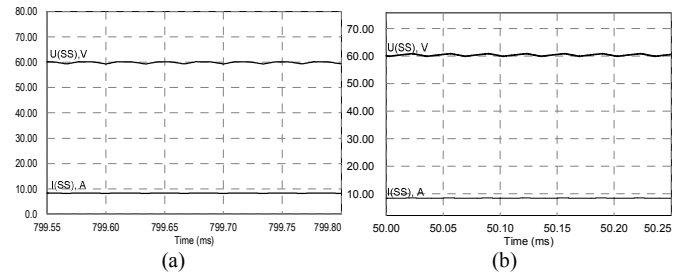


Fig. 12. Simulation results of the proposed converter during the SC discharging mode: SS side voltage ( $U_{SS}$ ) and current ( $I_{SS}$ ) at SC stack nominal (28.8 V) (a) and half of nominal (14.4 V) (b) voltage.

Despite the higher load power the variation of the SC voltage does not make it difficult to keep  $U_{DC}$ ,  $U_{TR}$  and  $U_{SS}$  on the predefined level (Fig. 11a and b). Also,  $U_{SS}$  and  $I_{SS}$  in both SC voltage extremes are the same (Fig 12a and b).

## IV. EXPERIMENTAL RESULTS

All the theoretical and simulation results were verified on the laboratory setup of the qZSI based bi-directional DC/DC converter. The operation and element ratings of the experimental setup are listed in Table I. The SC stack consists

of a series connection of two Maxwell Technologies SC modules (PCM14014) with a total capacitance value of 85 F, rated voltage  $U_{SC}=28.8$  V and equivalent series resistance of 20 m $\Omega$ .

### A. Charging Mode

At the very beginning of SC charging process the SC current  $I_{SC}$  can reach high values. To overcome this issue the SC stack was charged up to 12.5 V.

Fig. 13 shows that during the charging process the SS DC bus voltage  $U_{SS}$  is constant and the SC stack voltage  $U_{SC}$  increases up to the nominal value (28.8 V). At the beginning of charging process the SC stack current  $I_{SC}$  (Fig. 13) is around 135 A.

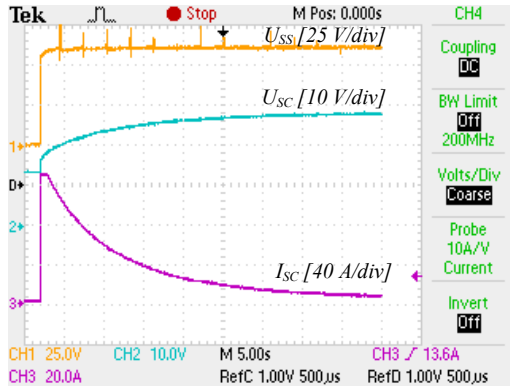


Fig. 13. Experimental waveforms of the charging process of the SC: SS DC bus voltage ( $U_{SS}$ ), SC stack voltage ( $U_{SC}$ ) and SC stack current ( $I_{SC}$ ).

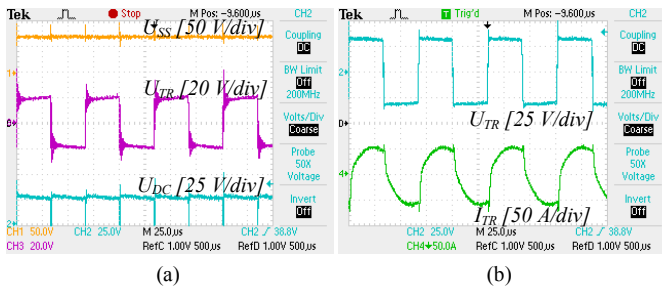


Fig. 14. Experimental waveforms during the SC charging mode: SS side voltage ( $U_{SS}$ ), transformer voltage ( $U_{TR}$ ), DC-link voltage ( $U_{DC}$ ) (a) and transformer voltage ( $U_{TR}$ ), transformer current ( $I_{TR}$ ).

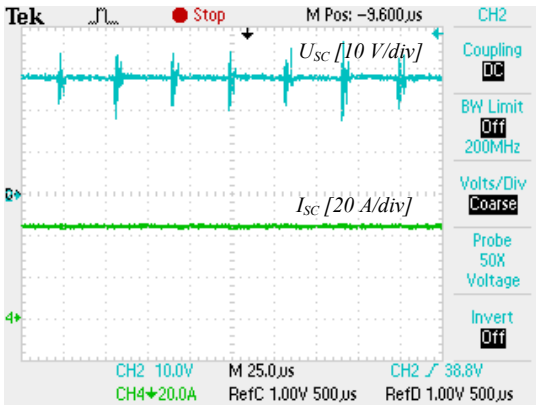


Fig. 15. Experimental waveforms during the SC charging mode: SC voltage ( $U_{SC}$ ) and SC current ( $I_{SC}$ ) during steady state.

Figs. 14 and 15 show that experimental waveforms of the proposed converter are in full agreement with the same waveforms that were made in simulation software.

### B. Discharging Mode

The experimental verification of the proposed converter was carried out to repeat the theoretical results obtained in the previous section.

#### Operation with 20 % of full load

The practical experiments at the power rating of 100 W of the proposed converter are presented in Figs. 16 - 18. As pointed out above, if the converter is supplied with the nominal or half of the nominal SC voltage ( $U_{SC} \dots 0.5U_{SC}$ ) (Fig. 16a and b) it can ensure the desired  $U_{DC}$ ,  $U_{TR}$  and  $U_{SS}$  at rated values (Fig. 17a and b) by the regulation of  $D_S$  of the qZSI.

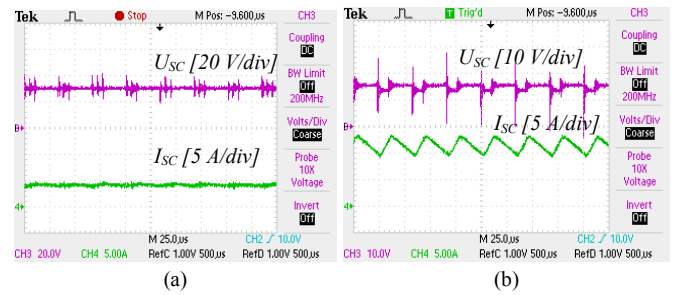


Fig. 16. Experimental waveforms of SC stack voltage ( $U_{SC}$ ) and current ( $I_{SC}$ ) at nominal (28.8 V) (a) and half of nominal (14.4 V) (b) value.

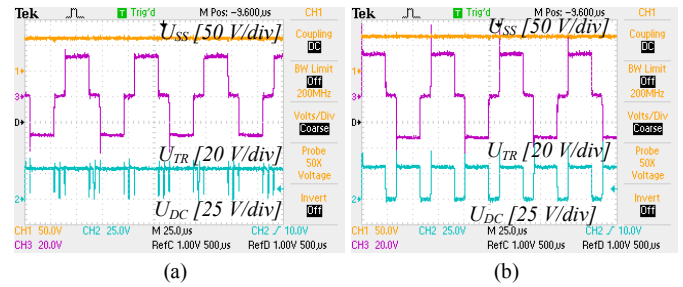


Fig. 17. Experimental waveforms of SC stack voltage ( $U_{SC}$ ), transformer voltage ( $U_{TR}$ ) and DC-link voltage ( $U_{DC}$ ) at SC stack nominal (28.8 V) (a) and half of nominal (14.4 V) (b) value.

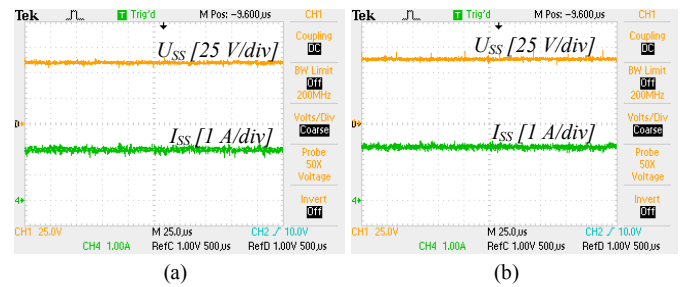


Fig. 18. Experimental waveforms of SS side voltage ( $U_{SS}$ ) and current ( $I_{SS}$ ) at SC stack nominal (28.8 V) (a) and half of nominal (14.4 V) (b) value.

It can be concluded that despite the SC voltage  $U_{SC}$  drop the desired SS side DC bus voltage  $U_{SS}$  level (Fig. 18a and b) can provide the same  $I_{SS}$  at equal load conditions.

## Operation with a full load

The second group of practical experiments was carried out at the power rating of the proposed converter of 500 W. Also, in this case all the results are in agreement with theoretical assumptions and simulation results, i.e. appropriate voltage boost can compensate the reduced SC  $U_{SC}$  (Fig. 19a and b) in order to obtain the desired voltage level on the DC-link, transformer and SS bus (Fig. 20a and b).

As a result of comparing the experimental waveforms in the conditions of 100 W and 500 W loading it can be concluded that the operation of the proposed converter is sufficiently adequate and it can successfully provide demanded voltage gain on the SS DC bus when it is necessary.

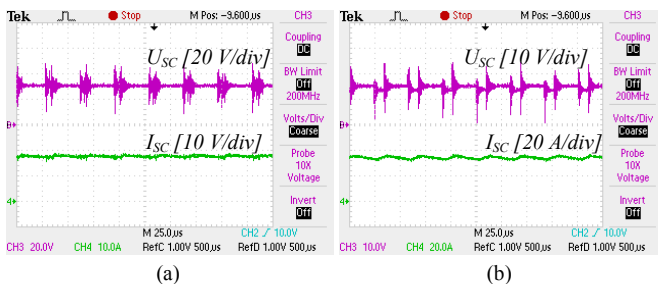


Fig. 19. Experimental waveforms of SC stack voltage ( $U_{SC}$ ) and current ( $I_{SC}$ ) at nominal (28.8 V) (a) and half of nominal (14.4 V) (b) value.

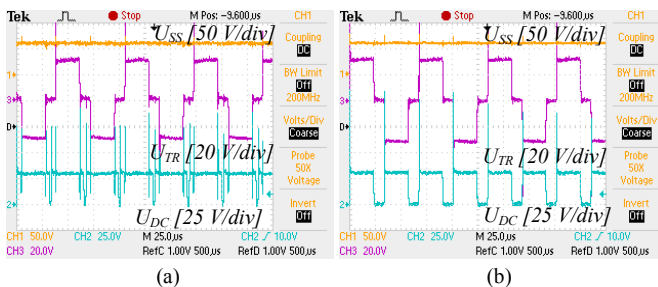


Fig. 20. Experimental waveforms of SC stack voltage ( $U_{SC}$ ), transformer voltage ( $U_{TR}$ ) and DC-link voltage ( $U_{DC}$ ) at SC stack nominal (28.8 V) (a) and half of nominal (14.4 V) (b) value.

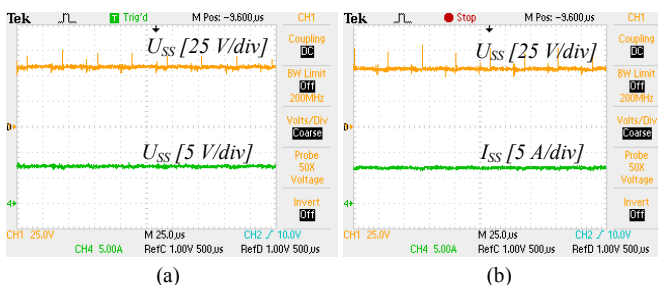


Fig. 21. Experimental waveforms of SS side voltage ( $U_{SS}$ ) and current ( $I_{SS}$ ) at SC stack nominal (28.8 V) (a) and half of nominal (14.4 V) (b) value.

## V. CONCLUSIONS

This paper describes a qZSI based bi-directional DC/DC converter for supercapacitor interfacing. The proposed converter was simulated in both operation modes. Also, an experimental verification was conducted on a 500 W laboratory prototype and compared with simulation results.

The most important generalizations and recommendations result in the following:

- to increase the efficiency of the proposed converter the cross-section of the conductors in the SC side should be properly selected;
- since some of the alternative energy sources (FC) are sensitive to the output current ripple, special attention should be paid to the selection of qZS-network inductors for the conditions of maximal boost;
- to escape additional input voltage boost on the account of semiconductor loss, power switches with the lowest forward voltage drop capability and qZS-network diodes with fast recovery time should be used;
- to reduce the high inrush current during the charging mode of the SC soft starters should be used.

The worst case efficiency of proposed converter is 87%.

It can be concluded that the proposed SC interfacing converter is a suitable and competitive solution for short term high-power energy storage devices in FC and/or PV powered residential energy supply systems.

## ACKNOWLEDGMENT

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