Experimental Study of High Step-Up Quasi-Z-Source DC-DC Converter with Synchronous Rectification

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***Abstract*—Quasi-Z-source DC-DC converters have attracted research interest due to their numerous advantages in emerging applications. However, they suffer from relatively low efficiency. This paper presents semiconductor loss breakdown of the quasi-Z-source DC-DC converter to show that conduction losses in semiconductors contribute most to overall losses. Synchronous rectification realized through replacement of diodes with N-channel MOSFETs was proposed to improve the converter efficiency in prior works. Our detailed experimental study of efficiency improvement with synchronous rectification was based on a 250 W prototype. Results were first obtained for replacement of diodes in the primary side only, then in the secondary side only. Finally, a converter that contains only controlled switches was evaluated. Efficiency curves measured were compared with those for the baseline diode-based topology. The experimental study was performed using operating points typical of photovoltaic module integrated converters.**

Keywords—DC-DC converter, synchronous rectification, quasi-Z-source, power losses, photovoltaic energy converter.

I. INTRODUCTION

The technology of galvanically isolated impedance-source DC-DC converters is an emerging trend in the modern power electronics [1]. It has gained popularity as a novel type of electric energy conversion alternative to current- and voltage-source converters. Among impedance-source converters, the quasi-Z-source (qZS) full-bridge DC-DC converter (Fig. 1) proposed in [2] suits best for renewable and alternative energy applications according to [3]-[5]. It features a wide input voltage regulation range performed within a single stage, continuous input current, immunity to shoot-through and open states of the inverter bridge, low inrush current, high control flexibility, etc. However, all these advantages are achieved at the cost of higher number of passive components and relatively low efficiency in emerging applications, which are usually associated with high input current and low input voltage values.

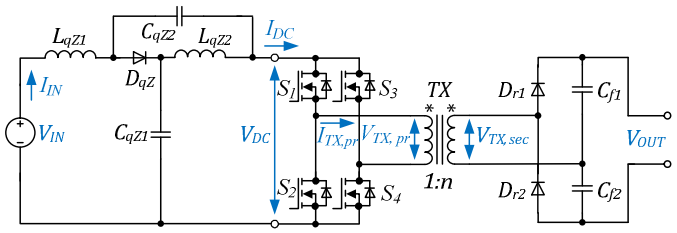

Fig. 1. Diode based quasi-Z-source full-bridge DC-DC converter.

Simulation study of the qZS DC-DC converter (qZSC) in [6] shows that conduction losses in semiconductors are the major cause of relatively low efficiency. Efficiency improvement through synchronous rectification was proposed and verified by help of simulation in [7]. It was suggested to replace diodes with N-channel MOSFETs in order to reduce conduction losses that are smaller in transistors than in diodes. Such replacement can be extremely advantageous even at higher cost related to the driver circuit implemented and additional losses for MOSFET driving. Fig. 2 shows an example of simplified calculation of conduction power losses in the Schottky diode with forward voltage drop $V_F = 0.6$ V, and in the MOSFET with on-state resistance $R_{DS(on)} = 9$ mΩ when they operate at constant current. Moreover, the MOSFETs feature the positive temperature coefficient of an on-state resistance and thus can be easily paralleled [8].

The simulation results in [7] show that the efficiency of the converter under discussion can be increased roughly by 2%. The aim of this paper is to verify this prediction experimentally. Section II describes the operating principle of the baseline converter and the simulation study of its semiconductor power losses. Then, three different realization possibilities of synchronous rectification are covered in Section III. Experimental measurements of efficiency for three topological variations of the case study converter are presented and compared with that for baseline diode based topology in Section IV.

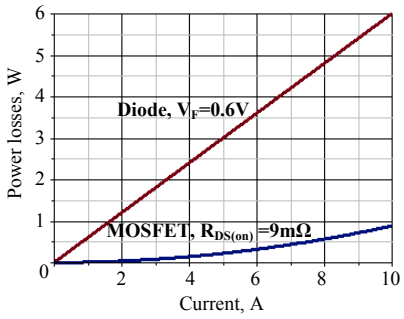

Fig. 2. Conduction losses in a diode and a MOSFET conducting constant current as functions of that current value.

II. Operating Principle and Semiconductor Power Losses of the Case Study Converter

A. Operating Principle of the qZS DC-DC Converter

The qZSC (Fig. 1) contains a qZS network, which comprises two capacitors C_{qZ1}, C_{qZ2}, two inductors L_{qZ1}, L_{qZ2}, and a single diode D_{qZ}. It couples input terminals and a full-bridge inverter $S_1 \ldots S_4$ that supply the step-up isolation transformer *TX* with rectangular bipolar voltage pulses. At the output side, this voltage is rectified and filtered with a voltage doubler rectifier (VDR), which contains two diodes D_{r1}, D_{r2} and two filter capacitors C_{f1}, C_{f2} that feed an output load. The converter performs voltage step-up at the input side through the PWM inverter control that contains shoot-through states in a switching sequence. The idea is to stabilize the inverter input voltage V_{DC} to maintain constant output voltage. Numerous shoot-through generation methods are available [9]-[12]. In the given case, the PWM with symmetrical overlap of active states seems to be the most appropriate, since its switching sequence contains no zero states that are virtually useless for control purposes due to the utilization of a VDR. Idealized voltage and current wave shapes of the given converter that features PWM with symmetrical overlap of active states are shown in Fig. 3.

This paper considers only continuous conduction mode, which requires proper dimensioning of the qZS network inductors [13]. Hence, the switching period *T* contains a combination of shoot-through states, which are used to step up input voltage and active states when energy is transferred from the input side to the output side through the isolation transformer *TX*. Shoot-through state is created by all four switches during the intervals (1) and (3) shown in Fig. 3. The qZS network limits the input current of the inverter I_{DC} at the level of cumulative currents of the qZS network, i.e. two times higher than the input current I_{IN}. The converter increases the energy stored in the qZS inductors, while the diode D_{qZ} is reverse biased. Cumulative duty cycle of the shoot-through states equals D_S. The other part of the switching period is dedicated to the active state, when one of the inverter diagonals supplies the isolation transformer with the voltage V_{DC} (intervals (2), (4) in Fig. 3). The qZS network behaves as a voltage source with the output voltage equal to the sum of qZS capacitor voltages. Transformer current is rising linearly with a slope defined by the leakage inductance of the isolation transformer. It charges the VDR capacitor C_{f1} or C_{f2} through the VDR diode D_{r1} or D_{r2}, respectively. Cumulative duty cycle of the active states equals $D_A = 1\text{-}D_S$. In case the input voltage of the converter equals the inverter nominal voltage, the converter operates without shoot-through states, similar to a conventional voltage-fed full-bridge converter (normal mode operation). The voltage across qZS network capacitors and the voltage gain of the converter *B* depend on the input voltage and shoot-through duty cycle [2]:

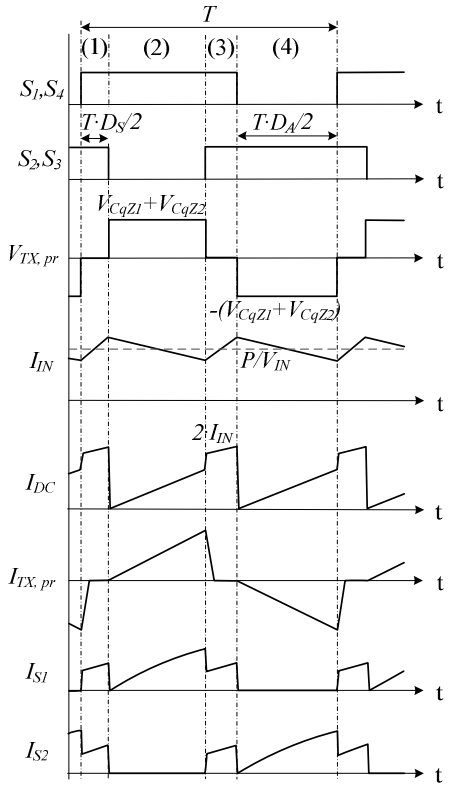

Fig. 3. Idealized current and voltage wave shapes of the qZSC.

$$V_{CqZ1} = \frac{1-D_S}{1-2\cdot D_S}\cdot V_{IN}\,,\; V_{CqZ2} = \frac{D_S}{1-2\cdot D_S}\cdot V_{IN}\,, \qquad (1)$$

$$B = \frac{V_{OUT}}{V_{IN}} = \frac{2\cdot n}{1-2\cdot D_S}\,, \qquad (2)$$

where *n* is the turns ratio of the isolation transformer.

B. Description of the Case Study qZS DC-DC Converter

Focus in this paper is on the MOSFET based qZSC designed as a photovoltaic module integrated converter. The operation range of the converter is limited by the rated operating power (*P*) of 240 W and the maximum continuous input current of 8 A. These limitations are common for interface converters for 60-cell solar panels. Usually, the maximum power point of such panes is within the range from 15 V to 30 V, depending on the weather conditions. For further studies, four operating points described in Table I were selected: three in the boost mode when shoot-through is utilized to step up the input voltage, which is lower than the nominal value, and one in the normal mode when the input voltage equals the nominal value. Evidently, the converter has to operate with different power and voltage step-up levels, while the input current remains constant for all operating points. All numerical simulations in this paper were performed using PSIM software with "Thermal module" add-on, which allows assessment of semiconductor power losses using datasheet parameters. Semiconductor devices described in Table II were used in the experimental prototype, while the simulation model implemented was based on their datasheet parameters. Table III presents the operating range, switching frequency and values of the passive components.

C. Analysis of Semiconductor Power Losses

First, the simulation study of semiconductor power losses was performed for the baseline diode-based qZSC for given operating parameters. Detailed distribution of semiconductor power losses for all operating points is presented in Fig. 4. It shows that the majority of losses present in the converter are conduction losses. It is evident that a qZS Schottky diode contributes most to semiconductor power losses relative to conduction losses, while its switching losses are close to zero. The conduction losses of the qZS diode (P_{DqZ}) are nearly constant, since they are defined by the forward voltage drop of the diode V_{F_DqZ} and the constant input current:

$$P_{DqZ} = V_{F\_DqZ} \cdot I_{IN} . \quad (3)$$

The conduction losses in the VDR diodes (P_{Dr}) change with the operating power linearly, since they depend on the forward voltage drop of the VDR diodes (V_{F_Dr}) and the output current, which depends on the operating power P linearly due to the constant output voltage V_{OUT}:

$$P_{Dr} = V_{F\_Dr} \cdot \frac{P}{V_{OUT}} . \quad (4)$$

The conduction power losses in the inverter MOSFETs (P_{Mcond}) contribute the last part to the semiconductor conduction power losses in the converter. They can be separated into two parts [6]:

$$P_{Mcond} = R_{DS(on)} \cdot P^2 \cdot \left(\left(\frac{4}{V_{IN}} \right)^2 \cdot D_S + 2 \cdot \left(\frac{8 \cdot n}{\sqrt{3} \cdot V_{OUT}} \right)^2 \right). \quad (5)$$

The first part is caused by the shoot-through state and depends on its duty cycle and the operating power. The second part is defined by the active state and depends only on the operating power value. Conduction power losses in the MOSFETs are rising slowly due to changes of both operating power and shoot-through duty cycle between the given operating points. It leads to their redistribution, while cumulative value changes slightly. These losses can be reduced if MOSFETs with lower on-state resistance ($R_{DS(on)}$) are used. However, they will require higher driving power and will provide slower switching dynamics due to higher parasitic capacitances.

Finally, the switching losses in MOSFETs are low due to low operating voltage and high dynamic performance of low-voltage MOSFETs. Their further reductions could require significant efforts without reasonable effect. Obviously, the simplest way to improve the efficiency of the converter considerably is to reduce conduction losses in the diodes. Synchronous rectification is commonly used to decrease semiconductor conduction losses. Three possible implementations of synchronous rectification in the qZSC are described in the next section.

TABLE I. OPERATING POINTS USED IN THE STUDY

Parameters	Test point			
	1	*2*	*3*	*4*
V_{IN}, V	15	20	25	30
I_{IN}, A	8	8	8	8
Voltage step-up (V_{DC} /V_{IN})	2.0	1.5	1.2	1
P, W	120	160	200	240

TABLE II. SPECIFICATIONS OF SEMICONDUCTORS USED IN THE STUDY

Component	Type	Specifications
$S_1 \ldots S_4$, S_{qZ}	Vishay Si4190ADY	V_{DS}=100 V; $R_{DS(on)}$=8.8 mΩ I_D=18.4 A, Q_g=20.7 nC, R_g=2.2 Ω
D_{qZ}	Vishay V60D100C	V_{RRM}=100 V; V_{F_DqZ}=0.66 V $I_{F(AV)}$=2x30 A (common cathode)
D_{r1}, D_{r2}	CREE C3D02060E	V_{RRM}=600 V; V_{F_Dr}=1.8 V $I_{F(AV)}$=4 A
S_5, S_6	ROHM SCT2120AF	V_{DS}=650 V; $R_{DS(on)}$=120 mΩ I_D=29 A, Q_g=61 nC, R_g=2.5 Ω

TABLE III.
GENERALIZED OPERATING PARAMETERS OF THE CONVERTERS

Parameter	Symbol	Value
Input voltage range, V	V_{IN}	15…30
Maximum input current, A	I_{IN}	8
Nominal DC-link voltage, V	V_{DC}	30
Output voltage, V	V_{OUT}	240
Switching frequency, kHz	f_{sw}	100
Operating frequency of the qZS-network, kHz	f_{qZS}	200 ($2 \cdot f_{sw}$)
Transformer turns ratio	n	1:4
Leakage inductance of the transformer, µH	L_l	0.5
Magnetizing inductance of the transformer, µH	L_m	30
Capacitance of qZS capacitors, µF	C_{qz1}, C_{qz2}	26.4
Inductance of qZS inductors, µH	L_{qz1}, L_{qz2}	22
Capacitance of output capacitors, µF	C_{f1}, C_{f2}	2.2

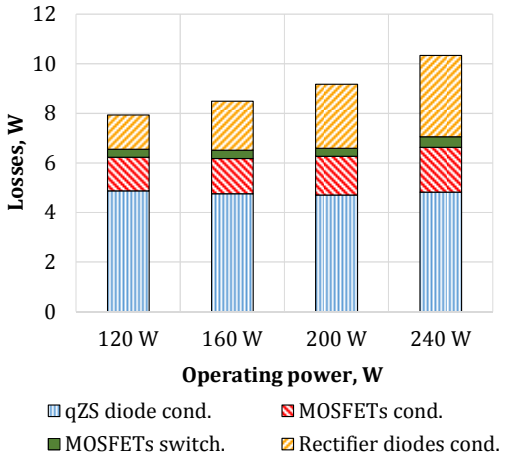

Fig. 4. Estimated semiconductor power loss breakdown.

III. Realization of Synchronous Rectification

A. qZSC with Synchronous qZS Network

The semiconductor power loss breakdown (Fig. 4) shows that diode D_{qZ} in the qZS network contributes from 49% to 64% of the conduction losses, depending on the operating point. These results were obtained for a Schottky diode, which is the most advantageous type for step-up converters that handle low voltage and high current at the input side. Nevertheless, it features considerable conduction losses, while its switching losses can be neglected. The qZS network diode D_{qZ} can be replaced with an N-channel MOSFET that is controlled synchronously with inverter switches in order to increase the converter efficiency, as shown in Fig. 5.

Control principle for that topological variation is shown in Fig. 6. Realization of synchronous rectification does not change the operating principle of the converter, while its efficiency can be improved. In the boost mode (Fig. 6*a*), the qZS MOSFET S_{qZ} must be turned off in the shoot-through state to prevent short-circuiting of the qZS capacitors. Hence, the dead-time of a proper duration must be utilized to avoid the failure and consequently, ensure high efficiency. Usually it is up to 100 ns for low-voltage MOSFETs. In the normal mode (Fig. 6*b*), the qZS MOSFET must be turned-on continuously to achieve the best performance.

A body diode of the qZS MOSFET conducts current during dead-time periods. Its dynamic performance is worse than that of the Schottky diode. Thus, effect from the implementation of the qZS MOSFET will be somewhat diminished by the switching losses of the body diode, mostly caused by the reverse recovery processes. Also, forward voltage drop of the body diode is higher than that of the Schottky diode, which results in additional conduction losses during the dead-time. Thus, the dead-time should not be overdimensioned. These drawbacks can be avoided if a small Schottky diode is connected in parallel to the qZS MOSFET to shunt its body diode [8].

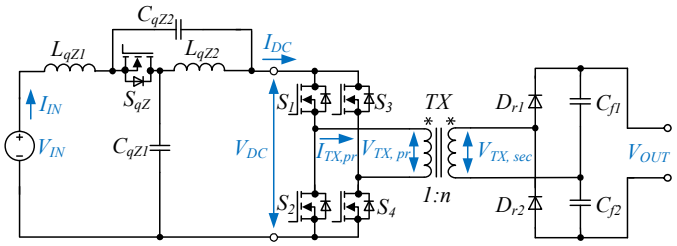

Fig. 5. Modified qZSC with the synchronous qZS network.

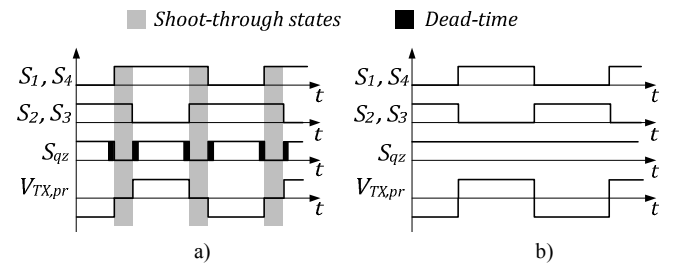

Fig. 6. Control principle of the qZSC with the synchronous qZS network in: a) the boost mode, and b) the normal mode.

B. qZSC with a Synchronous (Active) VDR

The conduction losses in the VDR diodes can be reduced in the same manner as in the qZS network, as shown in Fig. 7. In the baseline topology, the SiC Schottky diodes are common in the VDR due to their negligible switching losses, which is essential for the output high-voltage side of a high-frequency converter. To improve the efficiency of the VDR, high-voltage MOSFETs with low on-state resistance are required. Si superjunction (SJ) MOSFETs, like CoolMOS from Infineon, and SiC MOSFETs feature low enough resistance. Overall performance of the SiC devices is better than that of Si counterparts [15]. The Si SJ MOSFETs have high reverse recovery charge and parasitic capacitances, which leads to high driving power and switching losses [14]. Moreover, reverse recovery time of SiC MOSFETs is smaller by a factor of ten than that of the Si MOSFETs. Thus, they were selected for our further experimental study. The control principle for the topological variation with a synchronous VDR is shown in Fig. 8. It utilizes dead-times to avoid short-circuiting of the VDR capacitors. Switching losses of high-voltage switches are higher than those of low-voltage ones. Thus, reduction of conduction losses in the VDR will be affected by additional switching losses.

C. Full-Synchronous qZSC

The concept of a full-synchronous qZSC is derived by a combination of two topological variations described in this section above. The topology (Fig. 9) contains seven fully controlled switches. It has to combine benefits of the previous two topologies. Moreover, it can provide bidirectional power transfer [16]. All additional MOSFETs are controlled synchronously with inverter switches and utilize dead-time, as shown in Fig. 10. The dead-time of the qZS MOSFET S_{qZ} is avoided in the normal mode to improve the overall converter efficiency. At the same time, the VDR MOSFETs S_5, S_6 require dead-time for proper operation in both modes.

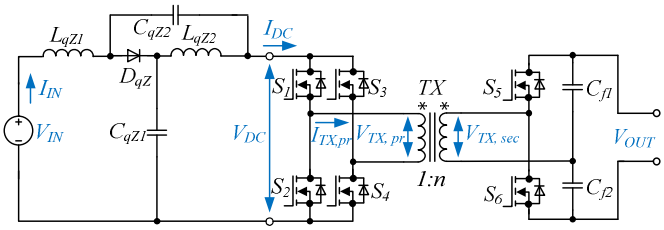

Fig. 7. Modified qZSC with a synchronous VDR.

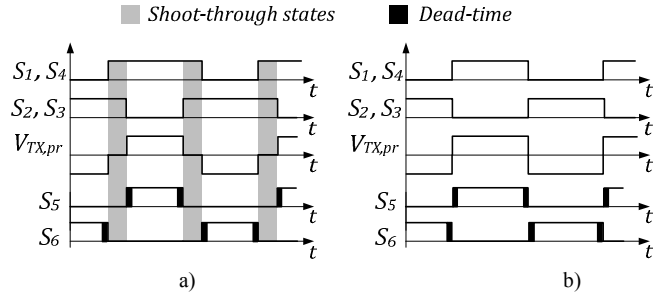

Fig. 8. Control principle of the qZS DC-DC converter with a synchronous VDR in: a) the boost mode, and b) the normal mode.

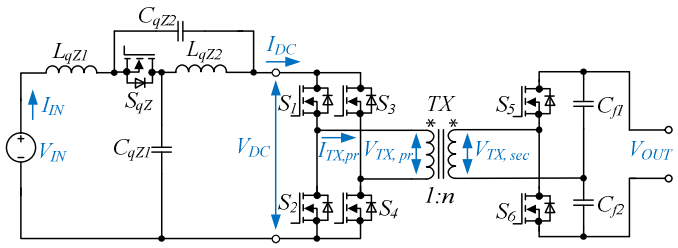

Fig. 9. Full-synchronous qZSC.

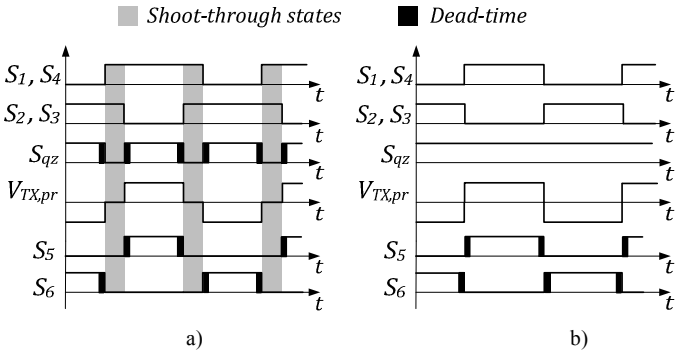

Fig. 10. Control principle of the full-synchronous qZSC in: a) the boost mode, and b) the normal mode.

IV. Experimental Results and Discussion

In this section results of our experimental study of three topological variations of the baseline qZSC are described. Specifications of all semiconductor devices used are described in Table II. First, the qZSC with the synchronous qZS network was tested. Current and voltage waveforms of the qZS MOSFET captured in the first operating point with the highest voltage step-up are shown in Fig. 11. The dead-time of 70 ns duration is evident there. This value was selected as a result of our preliminary experimental study. The measured efficiency curves for the qZSC with traditional and synchronous qZS networks are compared in Fig. 12. The converter efficiency rise is within the range from 0.9% to 1.7%, depending on the operating point.

A set of measurements similar those above was performed for the second topological variation, which contains the

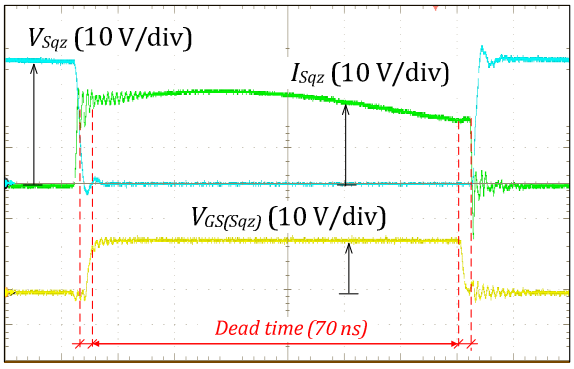

Fig. 11. Voltage and current waveforms of gating voltage, drain current and drain-source voltage of the MOSFET S_{qZ} captured in the test point with maximum shoot-through duty cycle.

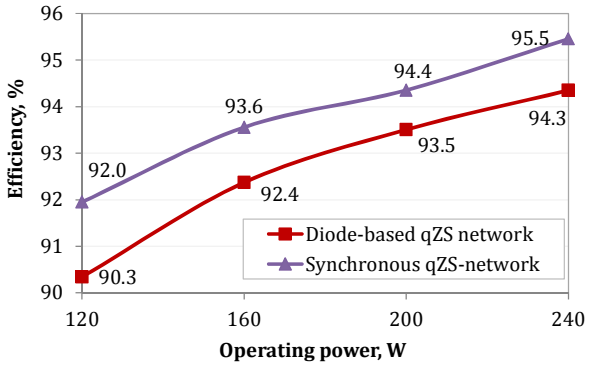

Fig. 12. Comparison of efficiencies measured in the case study qZSC with the diode-based and the synchronous qZS networks.

synchronous VDR. Voltage and current waveforms of the VDR MOSFET S_5 are shown in Fig. 13 for the normal mode. Hard turn-on of the switch, which results in very low efficiency rise is evident. Fig. 14 shows that the efficiency measured is up to 0.5% higher than that of the baseline converter, without consideration of driving losses.

Finally, the efficiency curve of the full-synchronous qZSC was obtained experimentally and compared with that of the baseline diode-based topology (Fig. 15). The cumulative efficiency rise is within the range from 1.1% to 1.9%, which is close to the efficiency rise by 2% predicted in [7].

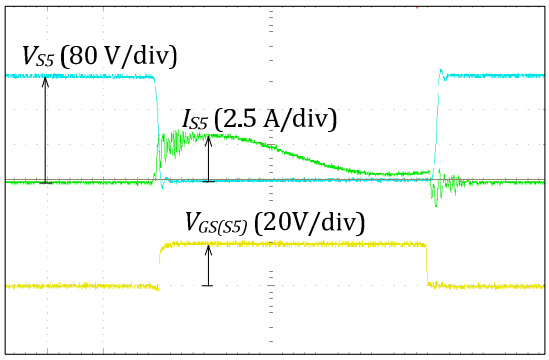

Fig. 13. Voltage and current waveforms of gating voltage, drain current and drain-source voltage of the MOSFET S_5 captured in the normal mode.

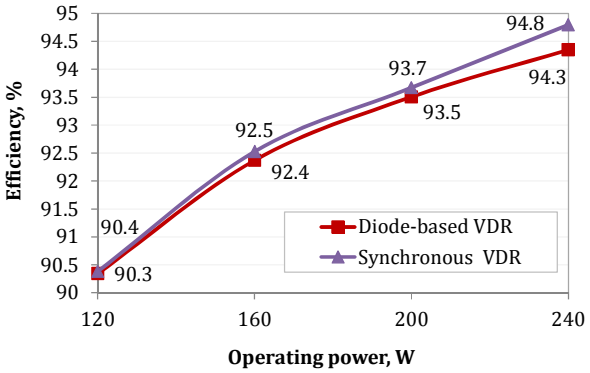

Fig. 14. Comparison of measured efficiencies of the case study qZSC with the diode-based and the synchronous VDRs.

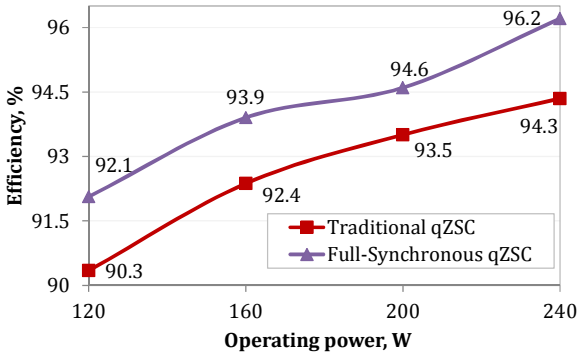

Fig. 15. Comparison of measured efficiencies of the full-synchronous and the traditional qZSC.

From the experimental results presented in this section it is evident that synchronous rectification can improve the efficiency of the case study qZSC by up to 2%. However, losses in the control system and driving were not taken into account in the efficiency measured. It means that 0.5% efficiency rise, i.e. 1.2 W in the given case obtained with the synchronous VDR can be easily suppressed by the driving losses of two high-voltage SiC MOSFETs. From a practical point of view, only qZSC with the synchronous qZS network seems to be an attractive solution if the driving losses and the cost of realization are taken into account, while bidirectional power transfer is not required.

V. Conclusions

Focus in this paper was on the efficiency improvement of the galvanically isolated quasi-Z-source full-bridge DC-DC converter through the realization of synchronous rectification. The study was performed for four operating points typical for photovoltaic applications. Our simulation study showed that in the given case, semiconductor power losses contain virtually only conduction losses. Moreover, conduction losses in the diodes contribute around 80% of the semiconductor losses in all operating points, while they can be easily reduced if diodes are replaced with N-channel MOSFETs. Three possible ways to realize synchronous rectification were studied: synchronous qZS network, synchronous VDR, and full-synchronous qZSC.

Efficiency curves were measured experimentally for the three topological variations proposed and compared with the baseline topology. It is shown that all topological variations provide a rise in efficiency. However, the measurements did not take into account the power required for driving additional MOSFETs, which can also involve power losses. Thus, the qZSC with the synchronous qZS network was found to provide best performance at the lowest cost if the driving losses are considered. Therefore, it will be advantageous as a high-performance photovoltaic module integrated converter.

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References

[1] A. Chub, L. Liivik, and D. Vinnikov, “Impedance-source galvanically isolated DC/DC converters: State of the art and future challenges," 55th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON), pp.67-74, 14 Oct. 2014.

[2] D. Vinnikov, and I. Roasto,”Quasi-Z-source-based isolated DC/DC converters for distributed power generation,” IEEE Transactions on Industrial Electronics, vol.58, no.1, pp.192-201, Jan. 2011.

[3] L. Bisenieks, D. Vinnikov, and J. Zakis, “Analysis of operating modes of the novel isolated interface converter for PMSG based wind turbines,” International Conference on Power Engineering, Energy and Electrical Drives (POWERENG), pp.1-8, 11-13 May 2011.

[4] J. Zakis, I. Rankis, and L. Ribickis, “Comparative analysis of boost and quasi-Z-Source converters as maximum power point trackers for PV panel integrated converters,” IEEE 23rd International Symposium on Industrial Electronics (ISIE), pp.1991-1995, 1-4 June 2014.

[5] T. Jalakas, I. Roasto, D. Vinnikov, and H. Agabus, "Novel power conditioning system for residential fuel cell power plants," 3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), pp.578-585, 25-28 June 2012.

[6] R. Kosenko, L. Liivik, A. Chub, and O. Velihorskyi, “Comparative analysis of semiconductor losses of the galvanically isolated quasi-Z-source and full-bridge boost DC-DC converters,” Electrical, Control and Communication Engineering, vol.8, pp.5-12, 2015.

[7] L. Liivik, D. Vinnikov, and J. Zakis, “Simulation study of high step-up quasi-Z-source DC-DC converter with synchronous rectification,” 55th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON), pp.34-37, 14 Oct. 2014.

[8] R. Selders Jr., “Synchronous rectification in high-performance power converter design,” Power Designer: Expert tips, tricks, and techniques for powerful designs, no.112, pp. 1-7, March, 2008. [Online]. Available: http://www.ti.com/lit/an/snva595/snva595.pdf [Accessed: Feb. 21, 2015].

[9] I. Roasto, D. Vinnikov, J. Zakis, and O. Husev, “New shoot-through control methods for qZSI-based DC/DC Converters,” IEEE Transactions on Industrial Informatics, vol.9, no.2, pp.640-647, 2013.

[10] I. Roasto, D. Vinnikov, T. Jalakas, J. Zakis, and S. Ott, “Experimental study of shoot-through control methods for qZSI-based DC/DC converters,” 2010 International Symposium on Power Electronics Electrical Drives Automation and Motion (SPEEDAM), pp.29-34, 14-16 June, 2010.

[11] Y.P Siwakoti, and G. Town, “Improved modulation technique for voltage fed quasi-Z-source DC/DC converter,” Twenty-Ninth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), pp.1973-1978, 16-20 March 2014.

[12] Y.P. Siwakoti, Fang Zheng Peng, F. Blaabjerg, Poh Chiang Loh, G.E. Town, and Shuitao Yang, “Impedance-source networks for electric power conversion part II: review of control and modulation techniques,” IEEE Transactions on Power Electronics, vol.30, no.4, pp.1887-1906, April 2015.

[13] R. Strzelecki, and D. Vinnikov, “Models of the qZ-converters", Journal “Electrical Review” ISSN 0033-2097, vol.86, no.6, pp.80-84, 2010.

[14] D. Graovac, M. Purschel, and A. Kiep “MOSFET power losses calculation using the data-sheet parameters”, Infineon Application note, V1.1, July 2006.

[15] J. Rabkowski, D. Peftitsis, and H.-P. Nee, ”Silicon carbide power transistors: a new era in power electronics is initiated, ” IEEE Industrial Electronics Magazine, vol.6, no.2, pp.17-26, June 2012.

[16] D. Vinnikov, I. Roasto, and J. Zakis, “New bi-directional DC/DC converter for supercapacitor interfacing in high-power applications,” 14th International Power Electronics and Motion Control Conference (EPE-PEMC), pp. T11-38 - T11-43, 6-8 September 2010.