RIGA TECHNICAL UNIVERSITY

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MULTI-PLANAR VOLUMETRIC 3D VISUALIZATION SYSTEM MODEL ANALYSIS AND IMPLEMENTATION IN FPGA

Summary of the Doctoral Thesis

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DECLARATION OF ACADEMIC INTEGRITY

I hereby declare that the Doctoral Thesis submitted for the review to Riga Technical University for the promotion to the scientific degree of Doctor of Engineering Sciences (Electronics), is my own. I confirm that this Doctoral Thesis had not been submitted to any other university for the promotion to a scientific degree.

Krišs Osmanis(Signature)

Date:

This doctoral thesis has been written in English and contains an introduction, six chapters with conclusions, references, 67 figures and 22 tables with 141 pages in total. The list of references consists of 133 titles.

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Nomenclature

List of mathematical symbols (in order of appearance)

relative single optical shutter layer transmittance in transparent state η_{open} relative single optical shutter layer transmittance in scattering state η_{closed} optical shutter transient response (transparent to scattering state) t_{decay} optical shutter transient response (scattering to transparent state) t_{rise} optical shutter physical horizontal size (width) $d_{\mathbf{w}}$ optical shutter physical vertical size (height) $d_{\rm h}$ spatial light modulator number of horizontal pixels $N_{\mathbf{w}}$ spatial light modulator number of vertical pixels $N_{\rm h}$ spatial light modulator binary pattern rate $R_{\rm slmBin}$ spatial light modulator mirror reset time tslmRst light source luminous flux $\phi_{v_{source}}$ optical transmittance of light path optical elements $\eta_{\text{passiveElements}}$ number of depth layers (depth resolution) Nlavers distance between two sequential depth layers dlayers bits per color $N_{\rm bpc}$ number of bits per color, modulated with PWM method $N_{b_{pwm}}$ $N_{\rm b_{lsim}}$ number of bits per color, modulated with LSIM method spatial light modulator bit reset mode (for bits modulated with PWM method) $E_{pwmSlmGlobalRst}$ number of base colors $N_{\rm colors}$ depth blanking period length ratio to optical shutter transient response time $R_{\rm dbs}$ inter-layer blanking period length ratio to optical shutter transient response time R_{db} user observation angle $\varphi_{\rm obs}$ user observation distance d_{obs} refresh rate (volumetric frames per second) $R_{\rm fps}$ multi-planar screen emitted light (luminance) $L_{v_{screen}}$ color variance or number of colors N_{colVars} $N_{\rm volRes}$ volume resolution in voxels voxel volumetric density NvolDens 3D perception score N_{Score3D} time to show whole volumetric image $t_{\rm v}$ depth blanking time period tdepthBlanking total time period (or sum) of inter-layer blanking periods t_{layerBlanking} all layer active image time t_{active} single blanking period time for inter-layer switching $t_{\rm blanking}$ time to show single depth plane image t_{depth} time to modulate single color $t_{\rm color}$ time to modulate chosen bits with PWM method t_{perPwmBits} time to modulate chosen bits with LSIM method t_{perLsimBits} time to load and output single bitplane with PWM method t_{pwmBit} time to load and output single bitplane with LSIM method t_{lsimBit} time to load single bitplane to spatial light modulator through digital data inter $t_{slmLoad}$ face G_{screen} screen gain incident light to the volumetric screen (illuminance) $E_{v_{screen}}$ luminous flux reaching the volumetric screen $\phi_{v_{screen}}$

- $\eta_{\rm slm}$ optical transmittance of spatial light modulator (time based)
- $\eta_{\rm vs}$ optical transmittance of volumetric screen
- $\eta_{\rm vst}$ optical transmittance of volumetric screen (time based)
- t_{per} given time period for calculating luminous flux
- ϕ_{avg} average luminous flux in given time period
- Q_{pwm} luminous energy during PWM bits
- Q_{1sim} luminous energy during LSIM bits
- $N_{\rm volume}$ physical volume of the multi-planar screen
 - $N_{\rm size}$ binary size of a single volumetric image for given spatial resolution and color depth
 - $N_{\rm bw}$ required bandwidth for 3d image transfer, bits per second
 - N_{bwpp} DisplayPort 1.2 available data bandwidth
 - *f*_{sym} *DisplayPort 1.2* symbol clock (540MHz)
 - N_{lanes} DisplayPort 1.2 data lanes
- $N_{\text{bits}_{\text{DP}}}$ bus width or bits per lane, per symbol clock cycle (after deserializer)
- $N_{\rm bw_{video}}$ DisplayPort 1.2 available data bandwidth for volumetric video transfer
- N_{blanking} blanking period symbols per volumetric frame

List of Abbreviations

- 2D Two dimensions
- 3D Three dimensions
- BIOS Basic Input Output System
- BSLS Broad Spectrum Light Source
- BTS Bradley-Terry Score
- CAD Computer-Aided Design
- CAM Computer-Aided Manufacturing
- CRT Cathode Ray Tube
- DDR Dual Data Rate
- DDR3 Dual data rate three
- DICOM Digital Imaging and Communications in Medicine
 - DLP Digital Light Processing
 - DMA Direct Memory Access
 - DMD Digital Micromirror Device
 - DVI Digital Visual Interface
- EEPROM Electrically Erasable Programmable Read Only Memory
 - FIFO First-In First-Out
 - FMC FPGA Mezzanine Card
 - FPGA Field programmable gate array
 - FPS Frames per second
 - HBP Horizontal Blanking Period
 - HD High Definition
 - HDMI High Definition Multimedia Interface
 - IC Integrated Circuit
 - IEEE Institute of electronics and electrical engineers
 - IP Core Intellectual property FPGA core
 - ITU-R International Telecommunication Union, Radiocommunication Sector
 - JTAG Joint Test Action Group
 - LC Liquid Crystal
 - LCD Liquid Crystal Display
 - LCOS Liquid Crystal On Semiconductor
 - LED Light Emitting Diode
 - LSE Laser Surface Engraving
 - LSIM Light source intensity modulation
 - LUT Look-Up Table
 - MCU MicroController Unit
 - MEMS Microelectromechanical System
 - MSA Main Stream Attributes
 - MSB Most Significant Bit
 - NSLS Narrow Spectrum Light Source
 - OLED Organic Light Emitting Diode
 - PC Personal Computer
 - PCB Printed Circuit Board
 - PCIe Peripheral Component Interconnection express
 - Pixel Picture Element
 - PWM Pulse Width Modulation
 - RAM Random Access Memory
 - RGB Three base colors red, green, blue
 - RMS Root-Mean Square

- RX Receiver
- SDR Single Data Rate
- SDTV Standard Definition Television
 - SID Society of Informative Displays
- SLM Spatial Light Modulator

SODIMM Small Outline Dual In-line Memory Module

- TI Texas Instruments
- TLP Transaction Layer Packet
- TU Transfer Unit
- TX Transmitter
- UART Universal Asynchronous Receiver Transmitter
 - USB Universal Serial Bus
 - VBP Vertical Blanking Period
- VGA Video Graphics Array
- VHDL Very high-speed integrated circuits Hardware Description Language
 - XGA Extended Graphics Array

General Description of Work

Urgency of Subject Matter

Modern electronics devices (mobile phones, laptops, tablet PC to name a few) implement user interaction through a digital display. These displays are capable of showing two-dimensional images to the user. Adding a third dimension (depth) to the 2D images is the next step. There have been numerous approaches to creating a full light-field 3D volumetric display device.

The simplest 3D imaging visualizations are created by stereoscopic 3D technology that uses a binocular effect [1]. The popularity of different kinds of 3D visualizations is a growing trend in the modern world, since better technologies lead to better devices and a better user experience.

Consumer-level stereoscopic 3D has been around since 1922, when the movie "*The Power Of Love*" was shown to a public audience at the *Ambassador Hotel Theater* in *Los Angeles* [2]. Since then, the stereoscopic 3D technology has seen its ups and downs multiple times being forecasted as both perspective and declining in the movie market. Nowadays, however, almost any *Hollywood* blockbuster is produced not only in the usual 2D, but also in 3D.

Industrial and medical applications of 3D visualizations are also becoming more common. Stereoscopic 3D has gained a foothold in medicine, engineering and other disciplines. For example, [3] indicates the trend of medical imaging fields, [4] shows volumetric 3D application for medical imaging systems, [5] reveals attempts to visualize volumetric data sets on a 2D display.

Volumetric 3D is much more challenging from implementation and the technology point of view, for it requires much higher data transfer channels and a specific screen.

Several volumetric 3D image creation principles exist as shown in literature review (Chapter 1). This thesis focuses on volumetric 3D display implementation based on multiple planar depth layers (forming a volumetric screen). This 3D visualization principle is one of the few technologies existing in the world that is capable of displaying real time live images from its source.

Although the multi-planar volumetric 3D technology idea itself is not novel, this thesis approaches the subject by applying the scientific optimization method as well as state-of-the-art technologies and their implementation to achieve better parameters when compared to previous generation volumetric displays with higher refresh rates, deeper color depth, and brighter images. In other words, this research attempts to squeeze out maximum possible performance of this technology.

The importance and urgency of research work is defined by the perspective significance in the application field. This visualization system can be used in medical applications such as computer tomography, x-ray scanning, and others; security such as with airport luggage scanning; and all other applications where precise 3D visualization is required. *Philips Healthcare* and *RealView Imaging* has conducted an evaluation [6] that shows volumetric and holographic 3D to be a feasible addition to minimally-invasive cardiology procedures. *MarketsMarkets* released a market research report the Spring of 2015 [7] that indicates volumetric display market trends of volumetric technology displays to reach \$348.2 million in sales by the year 2020.

Objective of the Work

The main objectives of the work are:

- Development of a mathematical model for a multi-planar volumetric 3D visualization system to achieve balanced quality metric parameters (such as overall luminance, color depth and refresh rate) by a set of design and operational parameters of the system;
- Research for novel methods to increase quality metric or operational parameters of the system;
- Research and implementation of volumetric 3D image transfer options for real time volumetric video imaging by using state-of-the art available technology (solutions);

• Development of a complete 3D volumetric visualization system prototype based on multi-planar depth plane technology and a high-speed projection system.

Scientific Novelty and Main Results

The results and scientific novelty in this work are as follows:

- Creation of a mathematical model for a multi-planar volumetric 3D visualization system that allows various types of analysis of the given system;
- A novel light modulation method for use with a *Digital Light Processing* (DLP) based projection system a mixed light modulation method, in which light is modulated by a combination of both a spatial light modulator and light source intensity;
- Research, development and implementation of an innovative real time volumetric 3D image transfer protocol based on the *DisplayPort 1.2* video transfer standard;
- Implementation of the system in actual FPGA based hardware and development of various FPGA IP cores, such as a *DisplayPort 1.2* receiver and a DLP controller with additional synchronization with a volumetric screen and a light source;
- A demonstration unit of multi-planar volumetric display technology (device *X1405* under the *LightSpace* brand);

Theses to be defended

- 1. The developed system mathematical model allows analysis and simulations of the multi-planar volumetric imaging system and proves that the mixed light modulation method provides a better relative luminance for a defined color depth and a minimum refresh rate;
- 2. A real time (25+ frames per second) volumetric image transfer rate can be achieved by using the *DisplayPort 1.2* physical carrier and the developed volumetric image transfer protocol;
- 3. A complete 3D visualization system (signal transfer and processing) with at least 25 volumetric images per second (20 depth layers, XGA resolution, 24 bits per voxel) can be implemented in a single *Xilinx Virtex-6* or similar class FPGA;
- 4. Sufficient depth perception is achieved from 15 to 20 depth layers (1024×768 spatial resolution) for generic 3D volumetric scene observation applications.

Research Technique

The basis of this research is formed by the following research techniques:

- Analytic research methods are used in literature analysis and mathematical model creation;
- Numerical methods and simulations are used to assess the mathematical model and technology capabilities as well as to specify requirements for implementation of the volumetric imaging system prototype;
- Simulations are used extensively to simulate data transfer links, light source effectiveness, light modulation options, operational modes;
- Practical experiments with both existing development tools (a *Xilinx ML605* development kit with *Virtex-6 XCV6LX240T-1FFG1156* FPGA), as well as real designed and manufactured PCB boards with extended features;
- Industry standard methodology for the subjective assessment of the quality of television pictures is used for verification;

Research Object

The main research object is the entire multi-planar volumetric 3D visualization technology itself with the following features:

- A system mathematical model;
- Volumetric 3D video data transfer;
- Video signal processing and remapping in the visualization system;
- Volumetric image transformation from the digital domain to a visible 3D scene.

Practical Significance of the Research

The practical significance of the research involves the created volumetric visualization system's model and implementation.

The developed model allows a rapid assessment of the visualization system's possible operating conditions based on various input parameter sets (for example, assess the impact of choosing a different spatial light modulator).

The research has been carried out at the industry company *SIA EuroLCDs* research laboratory. One of the goals of the research has been development and implementation for manufacturability of a prototype unit of the 3D volumetric technology. This has been done successfully and a complete 3D visualization system demonstration device has been implemented, verified and is ready to be manufactured.

In addition to the research, implementation of the demonstration device required a design of multiple PCB boards, a mechanical structure, liquid crystal shutters and driving and signal processing.

Completed research and implementation work have been included in the patent application [8].

Approbation

Scientific results of the research have been published in the papers

- Osmanis, K. Optimum Driving Conditions Study for Digital Micromirror Devices. *Proceedings* of the 13th Biennial Baltic Electronics Conference, Estonia, Tallinn, 2012, pp 61.–64. Available: doi:10.1109/BEC.2012.6376815
- Osmanis, K., Valters, G., Osmanis, I. Development of Digital Uncompressed 3D Image Transfer Using Displayport 1.2 Video Standard for Volumetric 3D Imaging Applications. *International Conference on 3D Imaging (IC3D)*, Belgium, Liege, 2012, pp 1.–5. Available: doi:10.1109/IC3D.2012.6615132
- Osmanis, K., Valters, G., Osmanis, I. 3D Volumetric Display Design Challenges. 31st Norchip Conference, Lithuania, Vilnius, 2013, pp 1.–4. Available: doi:10.1109/NORCHIP.2013.6702001
- Osmanis, K., Valters, G., Osmanis, I. Light Budget Study for a Multiplanar Volumetric 3D Display. *International Conference on 3D Imaging (IC3D 2013)*, Belgium, Liege, 2013, pp 1.– 5.

Available: doi:10.1109/IC3D.2013.6732099

- 5. Osmanis, K., Valters, G., Osmanis, I. 3D Volumetric Display Concept. *Proceedings of electronic displays 2014 scientific conference*, Germany, Nuremberg, 2014, pp 1.–5.
- Osmanis, K., Valters, G., Osmanis, I., Misāns, P. PCIe and DisplayPort Based High Speed Volumetric 3D Video Output Card Implementation In FPGA. *Proceedings of the 14th Biennial Baltic Electronics Conference*, Estonia, Tallinn, 2014, pp 1–4. Available: doi:10.1109/BEC.2014.7320556
- Osmanis, K., Osmanis, I. Real-Time Volumetric 3D Imaging Technology. *Biophotonics*, 2016, vol. 23, April, pp 30.–33. ISSN-1081-8693. Available:http://www.photonics.com

Scientific results of the research have been included in the patent

1. Osmanis, I., Osmanis, K., Valters, G. Multi-planar volumetric real time three-dimensional dis-

play and method of operation. Patent application No. PCT/IB2015/057484.

Scientific papers and practical results have been presented and approbated in the scientific and industry conferences and workshops

- 1. "13th Biennial Baltic Electronics Conference", 2012, 3.–5. October, Tallinn, Estonia.
- 2. "International Conference on 3D Imaging 2012", 2012, 3.–5. December., Liege, Belgium.
- 3. "TechNet Nano 2013", 2013, 13th June, Jurmala, Latvia.
- 4. "Norchip-2013", 2013, 11.–12. November, Vilnius, Lithuania.
- 5. "AIEEE 2013 Advances In Electronics and Electrical Engineering", 2013, 26th November, Riga.
- 6. "International Conference on 3D Imaging 2013", 2013 3.–5. December, Liege, Belgium.
- 7. ,Electronic displays 2014", 2014, 26.–27. February, Nuremberg, Germany.
- 8. "14th Biennial Baltic Electronics Conference", 2014, October, Tallinn, Estonia.
- 9. "Display Week 2015 International Symposium, Seminar and Exhibition", Society of Informative Displays, San Jose Convention Center, 2015, 2.–5. June, San Jose, USA.
- 10. Prototype device demonstration in "Philips Healthcare", 2015, 3rd July, Eindhoven, Netherlands
- 11. Prototype device demonstration in "GE Vingmed", 2015, 12th August, Oslo, Norway.
- 12. Prototype device demonstration in state research program *SOPHIS* result and review seminar. *Institute of Electronics and Computer Science*, 7th October, 2015, Riga
- 13. "RTU 56th International Scientific Conference", 2015, 14.–16. October, Riga.

Structure of the Doctoral Thesis

Thesis outline consists of situation analysis (literature review), multi-planar visualization technology introduction and system model development, concluded by development of data transfer, implementation of system's controller in FPGA and user evaluation test. Table. 1 shows scientific publication relation to the thesis research parts.

The 1st chapter is the literature review that includes an industry overview, statement and proof of the problem, overview and assessment of 3D visualization system technologies. The chapter introduces various volumetric 3D technologies and the up-to-date status of key industry developers, presents the history of multi-planar volumetric 3D display technology and discusses various quality metrics and their importance in visualization systems.

The 2nd chapter presents a detailed overview and principle of operation of the multi-planar volumetric 3D display technology. Light modulation methods and the proposed novel mixed modulation method for the projection system are also introduced here.

The next chapters tackle the mathematical model – the problem statement, development and solution. The first part is the model input parameter introduction in the 3rd chapter where various system characterization parameters are defined and divided into their corresponding groups – nonconfigurable, configurable and user location parameters.

The second part of the mathematical model introduces the system's output parameters (in correspondence to quality metric parameters) and the relationship to input parameters (also known as the mathematical model) in the 4th chapter. Output parameters such as volume refresh rate, luminance and color depth are introduced and explained.

The final part of the model in the 5th chapter analyses of the system's model and parameter-based partial (local) optimization attempts of an output parameter for a given set of input parameters and defined boundaries (minimum or maximum) for other output parameters. Various input parameter impact to the output parameters and quality metrics as well as the usability of the novel mixed light modulation method are also presented.

Scientific publication research structure

Reference	Publication Name	Research
[P1]/[9]	Osmanis K. "Optimum Driving Conditions Study for Digital Micromirror Devices." // 13th Biennial Baltic Electronics Conference (BEC), 2012, pp. 61.–64. (IEEE).	system model
[P2] / [10]	Osmanis K., Valters G., and Osmanis I. "Development of Digital Un- compressed 3D Image Transfer using DisplayPort video standard for volumetric 3D imaging applications." // International Conference on 3D Imaging (IC3D), 2012, pp. 1.–5. (IEEE)	data transfer
[P3]/[11]	Osmanis K., Valters G., and Osmanis I. "3D Volumetric Display Design Challenges" // Norchip 2013, pp. 1.–4. (IEEE).	implementation
[P4] / [12]	Osmanis K., Valters G., and Osmanis I. "Light Budget Study for a Multiplanar volumetric 3D display." // International Conference on 3D Imaging (IC3D), 2013, pp. 1.–5.(IEEE).	system model
[P5] / [13]	Osmanis K., Valters G., and Osmanis I. "3D Volumetric Display Concept." // electronic displays 2014, Nuremberg, 2014.	implementation
[P6] / [14]	Osmanis K., Valters G., Osmanis I., and Misans P. "PCIe and Display- Port Based High Speed Volumetric 3D Video Output Card Implemen- tation in FPGA." // 14th Biennial Baltic Electronics Conference (BEC), 2014, pp. 1.–4.(IEEE).	data transfer
[P7] / [15]	Osmanis K., Osmanis I. Real-Time Volumetric 3D Imaging Technol- ogy. // Biophotonics. 2016, April, Vol. 23, pp. 30.–33. ISSN-1081- 8693.	implementation

Experimental results and the demonstration device are introduced in the 6th chapter. The chapter explains volumetric data transfer research and implementation using the *DisplayPort 1.2* standard and PCIe connection, the implementation of volumetric data manipulations for use with high-speed projection system and control of the projection system. The chapter also presents user evaluation results of the developed system.

Note that this thesis is written as per the *IEEE 1541-2002* standard for binary prefixes. Kb (or Kbit) means 1000 bits (10^3) , Kib (or Kibit) means 1024 bits (2^{10}) .

1 Overview and Assessment of 3D Visualization System Technologies

This section presents actual and up-to-date information about the 3D visualization system technologies over the world. The first part of the literature review covers an overview of the 3D visualization system (various technologies, developers and availability of such systems) while the second part focuses on assessment and quality metrics of such systems. This overview forms a basis and presents the need and importance of the completed research.

1.1 Volumetric Imaging Applications and Data Sources

The volumetric imaging system produces a true three dimensional image within a defined three dimensional space that is enclosed within some kind of boundary (for example, a volume filled with free air, solid medium, gas, plasma, etc.) where the image is formed.

Based on the boundary type, such a volumetric imaging system creates a three dimensional scene that can be observed from either all directions, front-view, top-view or other limited views. An ultimate 3D visualization system would produce full light-field visibility, where an observer could view the scene from any direction.

Volumetric 3D imaging systems could be used in various applications. *Langhans K., et al* [16] proposes that some of applications can be scientific visualizations, entertainment, computer aided design, medical imaging, air traffic control among others. *Gong X., et al* [17] discusses the medical applications. *RealView* and *Philips* [6] has already carried out experiments on using a real-time 3D holographic visualization to assist in structural heart disease procedures with positive results.

1.2 Volumetric 3D Technology and Developer Overview

One of the most comprehensive and up to date overviews of volumetric 3D technologies has been done by *Geng*, *J*. [1]. He classifies all 3D display technologies based on how the human eye perceives the 3D effect meaning binocular stereoscopic or auto-stereoscopic (multi-view 3D, volumetric 3D, digital hologram). Other significant overviews have been done by *Favalora*, *G.E.* in [18], *Holliman*, *N.S. et al* in [19] and *Hong*, *J.* in [20].

Geng's paper presents a systematic review of state-of-the-art 3D display technologies and developers. He also refers to the Latvian company "*SIA EuroLCDs*" (and through it, to the research work represented in this thesis) as one of the main volumetric 3D technology developers.

Several notable and successful volumetric image generation technologies are introduced in the next several pages.

1.2.1 Static Volume, Passive Screen

Volumetric visualization systems that has a static volume (without any moving parts) and passive screen (not producing light itself) are grouped in this section. The most notable technologies are:

- Solid state upconversion a volumetric image is created inside a medium that can be excited at the required spatial location using two laser beams.
- Gas medium upconversion similar to previous technology, a gas medium can be used for volumetric image generation.
- Laser scanning (to produce plasma) 3D Display this laser scanning 3D display technique is expanded to produce visible voxels in the air from plasma generated by a laser.
- **Reactive solid state cube display** a volumetric image is created by applying an infrared electromagnetic wave to spatial locations (voxels) that emit light.

1.2.2 Static Volume, Active Screen

Volumetric visualization systems that have a static volume and active screen (producing light itself) are grouped in this section. Most notable technologies are as follows:

- Voxel array: a 3D transparent cube with optical-fibre bundles a volumetric image is created by spatially placed optical fiber, and voxels are made from optical resin and are transparent in their quiescent state.
- Voxel array (*LED* matrix) a three dimensional physical cube is created from *LEDs*, which can also be expanded to a larger scale and represents a volumetric voxel display.
- Layered *LCD* stack the technology is based on multiple electronically switch-able optical shutters (for example liquid crystal (*LC*) layers) that are stacked. An image projector projects sequential sections of a 3D image onto the screens.

1.2.3 Swept Volume, Passive Screen

Volumetric visualization systems that have a swept volume (volume is physically dynamic) and a passive screen are grouped in this section. Most notable technologies are as follows:

- A sweeping screen and a *CRT* a combination of *CRT* television with a rotating screen to form a 3D display. An image from *CRT* is relayed with a mirror and prism system to the rotating screen.
- A varifocal mirror and high-speed monitor the system consists of a high-speed monitor and a varifocal (variable focus length) mirror that is vibrated by a woofer and synchronized to the monitor.
- A laser-scanning rotating 3D display this technology produces a volumetric image by deflecting a beam of coherent light (generated by a laser) to a rotating helical surface.
- A *DLP* based rotating 3D Display a rotating flat light diffuser is projected upon by a mirror relay system and a *DLP* projection system.

1.2.4 Swept Volume, Active Screen

The volumetric visualization system that has a swept volume and active screen is:

• A rotating *LED* array – initial implementation consisted of an electroluminescent panel with a high-speed light emitter array. The array is rotating around its vertical axis, placed on the side of the array. 3D volumetric images are formed within the swept volume by controlling the x-y addressing and the rotation of the panel.

1.2.5 Actual Industry Players

The previous section covered multiple volumetric 3D technologies, which have been developed over the last decades. Some of the technologies are still in active development although market research reveals that there is actually a limited number of vendors that offer readily available volumetric display technology.

Key players of the volumetric 3D market nowadays are summarized on Table 1.1. The table shows that only one company, *Holografika*, publicly offers a volumetric display product line. The rest of the products by other companies are mostly still under development.

One reason for the lack of real products on the market could be scientific and technical challenges for implementing a visualization system that matches or outperforms well established 2D displays in terms of resolution, brightness, and image quality. Although volumetric image introduces naturally perceivable depth cues, other parameters should be similar to existing imaging systems and thus far, this has proven to be a challenge.

1.3 Quality Metrics of Visualization Systems

To understand, assess and compare the quality of various visualization systems (2D and 3D), industry standard quality metrics should be used. For various applications, quality metrics are used to characterize perceivable visualization effects for the user (for example, resolution and contrast).

Active developers of volumetric and glass-less 3D technologies

Company	Latest activities					
Toshiba	Hyper Viewer glasses-free display technology still under development					
	[21]. Additionally, Toshiba is working on software for better perception of volumetric medical data sets (<i>Voxar 3D</i> workstation) [22].					
3DIcon	Development of <i>CSpace</i> 360 degree 3D display [23] is in progress. <i>CSpace</i> will offer high resolution full color true 3D images.					
Realview Imaging	Israeli based company [24] is developing a holographic based floating volumetric image display. This company presents videos of working prototype and clinical cases.					
Holografika	Hungarian company [25] has released various holographic 3D displays; for example, <i>HoloVizio 80WLT, HoloVizio 722RC</i> .					
Burton Inc	Japanese company [26] is working on a 3D display technology based on the plasma emission phenomenon.					
Voxon	Startup in California [27] is developing a <i>Voxiebox</i> tabletop volumetric display system that is based on an up-down vibrating screen.					
Holoxica	England based company [28] is developing a dynamically changeable holographic display, currently third generation that will allow indepen- dently addressable voxels in space.					
Zebra Imaging	Located in Texas, this 3D holographic and motion display company [29] is working currently on the dynamic motion display <i>ZScape</i> .					
LEIA 3D	Startup company [30], located in California, is developing a 5.5" screen with a volumetric 3D effect based on holographic technology [31].					

The report Assessment of Display Performance for Medical Imaging Systems [32] by American Association of Physicists in Medicine overviews various existing display performance, their safety and evaluation standards for medicine and consumer grade display systems: SMPTE RP 133-1991, NEMA-DICOM Standard (PS 3), DIN V 6868-57, ISO 9241 and ISO 13406.

These standards and practices cover different aspects of display system assessment and compliance checking based on similar quality parameters: luminance, resolution, grayscale and color reproduction among others. These quality metric parameters are analyzed in more detail in the following subsections.

1.3.1 Resolution

Display system resolution characterizes the number of perceivable pixels or voxels in the display system. Resolution can be expressed in the form of (horizontal x vertical) pixels (e.g. (1280 x 1024)), total number of pixels (e.g. 2 MP – two million pixels or two megapixels) or in number of lines (e.g. 2 k, 2000-line display) [32].

Consumer grade 2D devices have a standardized set of resolutions (*Full HD*, *HD Ready*, 4 k, etc, usually with a pre-set aspect ratio). Medical grade displays have similar resolutions; for example, *Barco* diagnostics display *Coronis Uniti* (*MDMC-12133*) has (3840 x 2160) resolution.

The volumetric 3D resolution is similar to 2D systems with an additional z-axis number of voxels.

1.3.2 Refresh rate

System manufacturers such as *Barco* and *NEC* do not list a display system's refresh rate parameter rather, only the available image update rate is displayed based on the connection standard. The refresh rate as a stand alone parameter is mentioned in [32]. The display system itself should provide a flicker-free image and a minimum of around 55 Hz for 2D displays. This corresponds to the *CRT* type displays that has 50 or 60 Hz refresh rate.

1.3.3 Luminance

Luminance is one of the primary display system evaluation parameters. According to the *Barco* white paper on the differences between consumer grade and medical grade displays [33], consumer grade display systems usually have a maximum luminance of approximately 250 to 300 cd/m² while medical grade displays can reach up to 1000 cd/m². For example, *Barco* diagnostics display *Coronis Uniti (MDMC-12133)* has a *DICOM* calibrated maximum luminance of 1000 cd/m². The *American Association of Physicists in Medicine* [32] states the values for consumer grade to be around 100 cd/m² and high-luminance systems up to 600 cd/m². Both sources agree that luminance is an important parameter for display systems used in medical diagnostics and should be as high as possible.

1.3.4 Bit depth

Bit depth refers to a maximum number of simultaneously displayable gray levels. Consumer grade display systems usually have up to 8b grayscale. Professional and medical grade devices support bit depths up to 12 bit grayscale (*Barco Nio 5MP LED (MDNG-5221)*). High bit depth is essential in medical diagnostics, but for other applications the number may be lower.

Haidekker [34, 387.p] explains that biomedical image bit depths range from 8 bits (ultrasound, magnetic resonance, digital photography) to 14 (computer tomography) bits.

1.3.5 3D Quality

The literature review shows that there is no standard metric of 3D quality and this should be addressed due to the fact that various volumetric technologies produce images differently (as explained previously) and the images should be comparable in some way. Some attempts to measure quality of 3D imaging systems have been carried out. For example, *Philips Research* [35] carried out a visual quality assessment of lenticular based 3D-displays (auto-stereoscopic 3D).

For volumetric imaging systems parameters such as voxel density (number of voxels per volume), observation angle, and the number of users can be used to characterize the quality of 3D. In addition, the 3D reconstruction quality is characterized by the screen technology itself.

1.4 Summary and Conclusions

Existing volumetric imaging system assessment and quality metric parameter values are not widely available possibly due to the fact that most technologies are still in the prototype stages with the exception of the *Holografika* display systems (78M pixel 3D resolution, 24b (3x8b) colors, 300 cd/m^2 luminance) [25].

In order to implement the multi-planar volumetric visualization system, it is required to achieve comparable parameters to 2D display systems. This is also emphasized by preliminary meetings with *Philips Healthcare* [36] and *GE Medving* [37] medical system engineers. Reports of the *Lightspace Technologies DepthCube z1024* volumetric system demonstrations in 2004 also showed similar results with users looking for a high-contrast, high-brightness and flicker-free volumetric imaging system and existing solutions have not yet achieved this stage.

Thus, it is important to achieve a satisfying set of quality metric parameters for the volumetric 3D visualization system.

The following steps have to be carried out to solve the problem:

- Define the system architecture (key elements) and the operational principle. Propose novel ideas for light modulation methods as initial research work has shown that classical light modulation methods do not yield satisfying luminance / refresh rate / bit depth trade off results.
- Introduce the system parameters and the output (objective) parameters;
- Devise system mathematical expressions and model for output parameters;
- Incorporate light modulation methods and analyze the system model in order to maximize luminance while maintaining flicker-free refresh rate;
- Implement an experimental device and carry out a user evaluation test to verify the results.

2 Multi-planar 3D Visualization System Principle of Operation

This multi-planar 3D visualization method creates volumetric images (with real spatial coordinates) using a stack of electrically addressable and switch-able light diffusers (optical shutters) that are placed into the depth axis from the user point of view. The detailed exploded view is shown in figure 2.1. Five optical shutters are located one after another sequentially on the z axis at discrete positions (z = 0, z = 1, z = 2). These z coordinates then translate into real-life coordinates, for example: $z0_1 - z_0 = 10$ mm.

The volumetric image is created by projecting 2D images (slices of the 3D image) on a multiplanar screen, similar to as rear-projection displays, with the difference being that the screen consists of a number of planes rather than a single plane.



Figure 2.1: Multi-planar display with five depth planes schematic exploded view.

The projection system and the multi-planar screen are synchronized in such manner that at any single given moment, one shutter is in scattering state and the projected slice of the 3D image is visible on the shutter. All other optical shutters are in a translucent state. At the next moment, the next shutter is placed in a scattering state while the previous shutter is placed in a translucent state, and the next slice of the 3D image is visible on the next shutter.

This author proposes that a system model will help to find a suitable input parameter combination set for the required output parameters (such as the volumetric refresh rate and luminance). In order to create a system model, a detailed description of the projection system and the light modulation methods are required first.

2.1 Architecture Overview

The 3D visualization system is compromised of two key elements – a multi-planar volumetric screen and a projection system. Furthermore, the volumetric data source is also required in the system to provide the volumetric 3D video data. Functional architecture is depicted in Figure 2.2. The whole system is driven and synchronized by a controller that can be implemented in either a microprocessor (MCU), a field programmable gate array (FPGA) or in similar functionality integrated circuits.

Architecture elements are real physical devices that have a set of physical, configuration and operational parameters, which control the utilization of the device, such as the resolution of spatial light modulator or the multi-planar screen depth resolution.



Figure 2.2: Architecture overview of 3D visualization system.

2.2 Spatial Light Modulator and Light Source

The projection system's key component is the digital video pixel conversion to optical, visible pixel. This is done by spatial light modulator (SLM) in combination with light source and light modulation method.

2.2.1 Spatial Light Modulator

SLM is a miniature light-reflective microdisplay where each pixel acts as a reflective element or a mirror. Each element can be set to on or off state, similar to an optical switch. An array of the mirrors, set in the required positions, is called a binary pattern. Such microdisplays can achieve high binary pattern rates since the whole pattern can be loaded and switched on at the same time.

Two common commercially available SLM technologies are the *Digital Micromirror Device* (DMD) (a part of *Digital Light Processing* (DLP) chipset), manufactured by *Texas Instruments*, and the *Liquid Crystal on Semiconductor* (LCoS), originally developed by *General Electric* [38]. When comparing DMD and LCoS by the pattern switching speed, the DMD comes out as the clear winner. This is due to the fact that *William* [39] from *JVC North America R&D Center* reports a 12 ms response time for LCoS that corresponds to 83 grayscale modulated frames per second and therefore slower, while *DMD7000* [40] offers 32,552 binary patterns or 127 8-bit grayscale modulated frames per second using the pulse width light modulation method and is therefore faster.

Let us use the *Texas Instruments DLP7000* [40] mirror array as example to analyze the data interface. This is part of *DLP4100* chipset [41] and the data interface is executed through the *DLPC410* interface controller. *DLP7000* houses 768 rows, each with 1,024 mirrors (1024×768 pixels), grouped in 16 blocks of 48 rows. The data can be written to any row that is not currently being reset. Each 48 row block has its own reset command (applied through block command interface) and it initiates the mirror deflection process (mirrors physically toggle to the required positions). The process takes several microseconds, during which time no new data can be loaded to the corresponding blocks.

Applying the reset command to all blocks at the same time is called a global pattern output mode. The resetting of blocks separately is called the phased pattern output mode. The phased mode allows higher overall pattern output rates. This is because data can be continuously loaded to the blocks that are not in reset and mirror settling state. [40] states that for *DLP7000*, the highest rate of patterns per second can be achieved by resetting blocks in groups of four (also called – quads).

2.2.2 Light Sources

Several configurations and combinations of light source and light path elements that can be used with SLM are:

- 1. Broad spectrum light source (BSLS), color splitting with rotating wheel and single SLM, appears in [42, s. 2.1]. Colors are time multiplexed;
- 2. Broad spectrum light source, color splitting prism and three SLM, appears in [43, s. 3.2]. Colors are optically multiplexed;
- 3. Narrow spectrum light sources (NSLS), no additional color splitting is required, single SLM, appears in [42, s. 5.1]. Colors are time multiplexed;
- 4. Narrow spectrum light sources and three SLM, appears in [44]. Colors are optically multiplexed;

A broad spectrum light source implies a wide visible spectrum (white) light source, such as a xenon arc lamp. A narrow spectrum implies representation of the required primary colors most commonly red, green and blue.

Red, green, and blue colors are chosen as the primary colors for additive color mixing. This is based on the theory that the human eye is trichromatic (*Young-Helmholtz* theory) as explained by *Gegenfurtner* in [45]. Such a three-primary color additive mixing is usually implemented in display technologies such as CRT and LCD.

2.3 Light Intensity Modulation Principles

Light intensity modulation resulting luminous energy (grayscale value) is an integral of luminous flux over a given period of time [46]. Grayscale modulation by SLM is achieved by using light modulation methods, as explained in [47] and colors are achieved by applying grayscale modulation to specific incident colors (red, green, blue). Grayscale modulation principles are used in passive liquid crystal displays as well [48]. *Brennesholtz* mentions only the pulse width modulation for DMD grayscale modulation [49, p.60].

Two common light modulation methods that can be used in the proposed projection system:

- 1. Binary pulse width modulation [50], carried out by the spatial light modulator while keeping light source luminous flux output constant. This modulation method is described by *TI* in patent [51], filed in 1991, along with the invention of DMD itself. A detailed timing diagram is depicted in Fig.4.1;
- 2. Light source intensity modulation, carried out by a fast response light source, while the spatial light modulator outputs constant a binary pattern of the corresponding grayscale bit. This method is also partially described in [52], still overall, a vague number of papers in [53] show application of light source intensity modulation for the projection systems. The chief reason for this could be that the projection systems usually require high brightness to produce high contrast images, and so far, dynamically dimmable light sources (such as LEDs) have not been used in such systems, except in so-called pico projectors. A Detailed timing diagram is depicted in Fig.4.2.

The two mentioned modulation methods can be combined within a single grayscale output sequence to form a new novel light modulation method – *Mixed Light Modulation Method*. Literature and patent analysis shows that such a light modulation method for projection system's have never been used or mentioned before.

2.3.1 Mixed Modulation

The mixed modulation implies that the combination of time based pulse-width modulation and intensity based light source intensity modulation is used to modulate the single pixel grayscale value.

The mixed modulation method is shown in Fig.2.3. The figure depicts the output of the grayscale pixel value with a 5-bit binary representation. The top of the figure shows a light source luminous flux waveform (two bits are source modulated, three bits are pulse-width modulated). Pixel[4..0] =



Figure 2.3: Mixed modulation sequences for various 5-bit wide pixel grayscale values.

"zzzzz" shows pixel grayscale value that is output, where "zzzzz" is the 5-bit binary representation of a pixel value. The figure also shows that light intensity remains at 100% during PWM bits and drops by half for each corresponding LSIM modulated bit. The bottom line shows corresponding bit time slots.

Some resemblance to the mixed modulation can be seen in [52], but [53], [48] and application information analysis lack proof for applying this technique to projection systems and SLM thus, it can be considered as a novel technique. The results of this modulation method application for the projection system is published in paper [9].

2.4 Summary

This section introduced the principle of operation for the 3D visualization system, presented several architecture options, introduced the spatial light modulator principle of operation and light modulation methods for use with SLM.

To form a basis for further system modelling and experimental implementation, projection system architecture must be chosen. In order to assess and evaluate the novel proposed mixed light modulation method, solid state NSLS light sources will be used combined with a single SLM in the first prototype (a single SLM system is easier and cheaper to build than three SLM systems and the researched and developed results can be transferred to three SLM configurations). This architecture decision forms a basis for further system modelling.

3 System Model and Input Parameters

Creation of a system model begins with defining various input parameters. Each architecture element is characterized by one or more parameters. In turn, these parameters are called input parameters as they define how the system is operating. Parameters are grouped by their corresponding architecture element and elements are grouped by their source – the ability to impact the element and parameter value. Three element groups are proposed:

- 1. Nonconfigurable parameters elements in this group are manufactured by industry companies (for example, the aforementioned *Texas Instruments*, *EuroLCDs* and others) and must be chosen from the available options;
- 2. Configurable parameters elements in this group can be directly controlled and chosen the in design phase or during operation by selecting one of the light modulation methods for example;
- 3. User location parameters elements in this group characterize where the user is located in regards to the visualization system. As shown in section 2.1 and Fig.2.2, the user is looking at the 3D visualization system's *Multi-planar screen* and the user's perceived quality of 3D image is directly influenced by his or her location.

3.1 Nonconfigurable Parameters

3.1.1 Optical Shutter

Optical shutters are characterized by their transient and optical parameters. Typical voltage driving waveform and transient response of LC shutters are depicted in Fig.3.1 [54] and [48].

The optical transient delayed response is shown as the decay and rise time of transmittance. The delayed response when switching the LC shutter from a highly transparent open state to a scattering state is known as decay time (t_{decay}) while the response when switching from a scattering state to an open state is known as rise time (t_{rise}). The switching of optical states is done by applying bipolar driving voltage as shown in the figure below.



Figure 3.1: Typical light transmittance switching based on applied drive voltage on liquid crystal shutter (not to scale).

Relative single layer open transmittance (η_{open})

This parameter defines the single optical shutter open state relative optical light transmittance. The ideal value of the parameter is 100 %, or complete loss-less light transmittance, as if in free-air. In reality, this parameter is not 100 % and a small amount of scattering exists even in its open state.

Relative single layer scattering state light transmittance (η_{closed})

The shutter's scattering state quality determines how well the projected image from the projector is diffused (or intercepted). This parameter is related to screen gain when calculating display luminance.

Single layer open-to-closed and closed-to-open switching time periods (t_{decay} , t_{rise})

This parameter is measured as the transient response time between 10 % of η_{closed} to 90 % of η_{open} . This time period is physically dependant on the applied electrical field per cm², the liquid crystal material, the thickness of a cell and other parameters [48].

In the 3D volumetric imaging system this response time must be taken into account so that the image is not blurred between layers by implementing the required blanking periods. Each blanking period reduces overall effective refresh rate and brightness.

Shutter physical dimension (horizontal and vertical size) (d_w, d_h)

Shutter horizontal and vertical size determines the visualization system's perceivable 3D image maximum width and height. It influences size and the reconstructed 3D image quality.

3.1.2 Spatial Light Modulator

SLM elements are introduced and explained in section 2.2.1 and from the input parameter point of view, the SLM characterizing parameters for the 3D visualization system are resolution, binary pattern rate per second and transient idle periods.

SLM resolution (horizontal and vertical pixels) (N_w,N_h)

The spatial light modulator resolution is determined by the number of reflective elements (mirrors). Manufacturers make devices with industry standard resolutions (640x480, 1920x1080, ...) and aspect ratios (4:3, 16:9). The maximum values for both parameters in the real world are resolutions for displays such as 8K *Fulldome* (8192 x 8192) projectors used for instance, in a dome planetarium.

SLM binary pattern rate (*R*_{slmBin})

This parameter characterizes how many times per second binary patterns can be shown on an SLM surface including the loading and display time. This is usually defined by the SLM IC and its data bandwidth capability – its clock frequency, data bus width, words per clock cycle as well as the actual physical construction of the chip.

Realistic value range is 4,000 to 32,552 patterns per second; as such capable SLM exists at the moment that can be seen in [55].

SLM mirror reset time period (t_{slmRst})

The time period is based on the SLM physical construction (size of mirrors, weight). The value is usually noted in the datasheets. For *DLP7000* [41] the parameter is defined as $\approx 12.5 \,\mu$ s.

3.1.3 Light Source and Passive Light Path

Light source, SLM and the multi-planar screen are knotted together by a specifically light path. The main purpose of the light path is to collect light source emitted light, homogenize it, relay and focus it on SLM, relay and focus it to the projection lens and relay it to the multi-planar screen.

Light source luminous flux ($\phi_{v_{source}}$)

This parameter characterizes the power of the light source. Luminous flux of discrete color light sources can be characterized by a single luminous flux value. This is because colors are implemented by time multiplexing (explained in sec. 2.2.2) thus, the average of luminous flux values is used.

Optical elements ($\eta_{\text{passiveElements}}$)

For model purposes of this visualization system, optical light path elements are characterized with relative optical transmittance and are used for calculating display brightness. The required optical elements include: collection lenses, relay lenses, a homogenization rod, a prism and a projection lens.

3.2 Configurable Parameters

The system's configurable and operational input parameters can be directly influenced during implementation and operation of the visualization system.

3.2.1 Multi-planar Screen Construction

The multi-planar screen can be modelled with the number of depth planes and distance between each plane.

Number of depth planes (N_{layers})

The number of depth planes should be infinite to show the perfect 3D image. This is not possible due to the physical characteristics of an optical shutter. The minimum number of depth planes is two but fewer than 10 would result in a distorted volumetric image.

Distance between two sequential layers (d_{layers})

This variable defines physical distance of depth planes. The minimum distance between two layers is zero (in other words, the shutters placed side by side, and next to each other). The combination of the distance between each layer and a number of layers define overall depth size of the multi-planar screen. The depth size determines a possible depth perception effect.

3.2.2 Timing, Modulation and Color Parameters

This parameter group introduces input parameters that can be adjusted during real time operation of the visualization system. These parameters include the modulation method, color depth and blanking periods. The chosen light modulation method is determined by a configuration of bits per color in PWM bits and LSIM bits so that total bits per color is $N_{\text{bpc}} = N_{\text{bnym}} + N_{\text{blym}}$.

Number of PWM bits $(N_{\mathbf{b}_{pwm}})$

This input parameter represents the number of bits to be modulated with the pulse width modulation method. The parameter boundaries are from 1 to N_{bpc} .

Number of LSIM bits (N_{blsim})

This number represents the LSIM part of single color depth. Feasible values for this system model analysis are similar as for $N_{b_{nwm}}$.

PWM modulation bit SLM reset mode (*E*_{pwmSlmGlobalRst})

This parameter controls the pulse-width modulation bit timing period. This means PWM bitplanes are output to SLM using global or phased pattern output modes (shown in section 2.2.1). This value can take on only two values -0 and 1 (enable/disable global pattern mode) as shown in Eq. (4.7).

Number of base colors (N_{colors})

The number of base colors define possible color space. Although nowadays display systems usually offer a broad spectrum of colors, there may be applications where grayscale (single color) can also be used; for example, computer tomography can produce grayscale images.

Depth blanking period length ratio to shutter optical switching length (R_{dbs})

This timing parameter characterizes length of inserted blanking period between the last and the first volumetric depth layer. It is required to separate the first and the last image slices to avoid their overlapping (part of the first depth layer slice appears on the previous one – the last depth layer) thus, corrupting the reconstructed image. The optical shutter transient delay ratio to blanking period (defined as $R_{dbs} = \frac{t_{depthBlanking}}{\max(t_{decay}, t_{rise})}$) is used to define the blanking period.

Inter-layer blanking period length ratio to shutter optical switching speed (R_{db})

This timing parameter controls the length of the inserted inter-layer blanking period between each sequential volumetric slice. This is similar to the depth blanking period parameter, but is inserted between each consequential layer. Ratio is defined as $R_{db} = \frac{t_{blanking}}{\max(t_{decav}, t_{rise})}$.

3.3 User Location Parameters

The visualization system is perceived by a human being who observes the reconstructed 3D volumetric image. The exact location of the observer is important to the perceived quality of image thus, parameters defining placement are used.

Observation angle (φ_{obs})

Observation angle (φ_{obs}) is defined as an angle between the screen surface normal (0°) and the vector pointing at observer.

Observation distance (d_{obs}) .

The distance is defined as the observer's eye distance from the front of the multi-planar screen.

4 Objective Parameters and Mathematical Model

The visualization system performance is usually characterized by size, resolution, refresh rate, luminance, number of colors and other parameters. In order to maximize multi-planar volumetric display objective parameters, the main focus will be on refresh rate, luminance, color depth and the perceivable 3D image quality. The system's mathematical model is introduced in a top-down manner based on each objective parameter. Objective (output) parameters are:

- $R_{\rm fps}$ refresh rate (volumetric frames per second), $[R_{\rm fps}] = {\rm Hz}$
- $L_{v_{screen}}$ luminance, $[L_{v_{screen}}] = cd/m^2$
- N_{colVars} color variance or number of colors, $[N_{\text{colVars}}]$ = integer
- 3D image quality parameters:
 - N_{volRes} volume resolution, $[N_{\text{volRes}}]$ = integer
 - N_{volDens} voxel volumetric density, $[N_{\text{volDens}}]$ = integer
 - N_{score3D} 3D perception score, $[N_{\text{score3D}}]$ = integer

4.1 Volume Refresh Rate

Volumetric refresh rate frequency is a reciprocal of the required time period to show full volumetric image (including all volumetric depth layers, all blanking periods, each layers image and colors at the required color depth). This is shown in Eq. (4.1).

$$R_{\rm fps} = \frac{1}{t_{\rm depthBlanking} + t_{\rm layerBlanking} + t_{\rm active}}$$
(4.1)

where $t_{\text{depthBlanking}}$ – depth blanking time period;

 $t_{\text{layerBlanking}}$ – total time period or sum of inter-layer blanking periods;

 t_{active} – all layer active image time.

The depth blanking period length is defined by a ratio R_{dbs} to liquid crystal shutter open-to-closed or closed-to-open switching time as shown in Eq. (4.2):

$$t_{\rm depthBlanking} = R_{\rm dbs} \max(t_{\rm decay}, t_{\rm rise})$$
(4.2)

where R_{dbs} – ratio that defines depth blanking period length to shutter switching time period;

 t_{decay} – liquid crystal shutter decay time period;

 $t_{\rm rise}$ – liquid crystal shutter rise time period.

The whole volumetric image total inter-plane blanking period length is calculated as shown in Eq. (4.3). Each sequential depth layer except switching between the first and the last is summed together.

$$t_{\text{layerBlanking}} = (N_{\text{layers}} - 1) t_{\text{blanking}}$$
(4.3)

where $t_{\text{layerBlanking}}$ – single blanking period time for inter-layer switching;

 N_{layers} – multi-planar screen number of depth planes;

 t_{blanking} – blanking period between two sequential layers.

Inter-plane blanking is governed as a ratio to liquid crystal shutter open-to-closed or closed-toopen switching time period as shown in Eq. (4.4):

$$t_{\text{blanking}} = R_{\text{db}} \max(t_{\text{decay}}, t_{\text{rise}}) \tag{4.4}$$

where R_{db} – ratio that defines blanking period length to shutter switching time period.

Active volumetric image time (the time during which image is projected to the screen) is defined by the number of depth planes and the time it takes to modulate each 2D plane separately (2D image for that depth plane) as shown in Eq. (4.5).

$$t_{\text{active}} = N_{\text{layers}} t_{\text{depth}} \tag{4.5}$$

where t_{depth} – time to show single depth plane image.

Single 2D plane image time t_{depth} is defined by the time it takes to show a single 2D image with required pixel bit depth and number of colors. As the visualization system is built with a single DMD chip, all base colors are shown time sequentially, thus, the active period is defined as shown in expression (4.6):

$$t_{\rm depth} = N_{\rm colors} t_{\rm color} \tag{4.6}$$

where N_{colors} – number of colors used in system;

 $t_{\rm color}$ – time to module single color.

Single color modulation time is a sum of time periods required for PWM and LSIM modulations as shown in Eq. (4.7). This equation allows us to bring together previously presented light modulation methods.

 $t_{\rm color} = t_{\rm perPwmBits} + t_{\rm perLsimBits}$ (4.7)

where $t_{perPwmBits}$ – time period for modulating PWM bits;

 $t_{\text{perLsimBits}}$ – time period for modulating LSIM bits.

The time period for modulation of PWM bits is governed by a single bitplane time step and a required number of color bits to be modulated with PWM. The modulation time period is calculated by multiplying the time period required for a single bitplane modulation by the number of time steps. The number of required time steps for binary pulse width modulation is based on the required bit resolution and can be calculated by expression (4.8). For example, for eight color bits, the number of time steps are $2^{N_{\text{bpwm}}} - 1 = (N_{\text{bpwm}} = 8) = 2^8 - 1 = 255$.

$$t_{\text{perPwmBits}} = t_{\text{pwmBit}} \left(2^{N_{\text{bpwm}}} - 1 \right) \tag{4.8}$$

where t_{pwmBit} – time to load and output single PWM bitplane;

 $N_{b_{pwm}}$ – number of bits to be output with PWM modulation.

The time period for LSIM bits modulation is governed by a single bitplane time step and a required number of color bits by multiplication shown in Eq. (4.9). The number of required time steps for light source modulation is based on the required number of bits and is the same as number of bits. This is due to each bitplane being shown on SLM and meanwhile is modulated by a light source.

$$t_{\text{perLsimBits}} = t_{\text{lsimBit}} N_{\text{b}_{\text{lsim}}}$$
(4.9)

where t_{lsimBit} – time to load single LSIM bitplane;

 $N_{b_{lsim}}$ – number of bits to be output with LSIM modulation.

Time to load and show a single bitplane depends on SLM type and reset cycling. PWM bitplanes can be output by either phased or global reset mode and this setting is governed by parameter $E_{\text{PwmSlmGlobalRst}}$. PWM bitplane time calculation is shown in Eq. (4.10):

$$t_{\text{pwmBit}} = t_{\text{slmLoad}} + \left(E_{\text{PwmSlmGlobalRst}} t_{\text{slmRst}} \right)$$
(4.10)

where $E_{\text{PwmSlmGlobalRst}}$ – variable that can be either 0 or 1;

 t_{slmLoad} – time for loading a single bitplane (minimum bitplane time);

 $t_{\rm slmRst}$ – time it takes to reset and settle whole bitplane globally.

LSIM bitplane must be output with global resets, because whole bitplane needs to be shown at the same time, to modulate intensity of whole bitplane correctly, time calculation is shown in expression:

$$t_{\rm lsimBit} = t_{\rm slmLoad} + t_{\rm slmRst} \tag{4.11}$$

Time to load single bitplane to the SLM can be calculated by:

$$t_{\rm slmLoad} = \frac{1}{R_{\rm slmBin}} \tag{4.12}$$

where R_{slmBin} – Spatial light modulator binary patterns per second.

Spatial light modulator mirror reset and settling time is shown in expression:

$$t_{\text{slmRst}} = f(\text{SLM}) = 4.5 \,\mu\text{s} + 8 \,\mu\text{s} = 12.5 \,\mu\text{s} \text{ for DLP7000}$$
 (4.13)

All timing parameters regarding system's refresh rate output parameter have been unwrapped to the level of input parameters and the model can be used for analysis.

4.2 Luminance

Volumetric 3D visualization system luminance is the display's capability of producing quality and perceivable images. Luminance is dependent on multiple parameters such as single shutter quality, multi-planar screen construction, number of depth layers, spatial light modulator, viewing angle and more. Projection type screen luminance can be calculated by the formula given in [49, p. 327]:

$$L_{\rm v_{screen}} = \frac{E_{\rm v_{screen}}}{\pi} G_{\rm screen} \tag{4.14}$$

where $L_{v_{screen}}$ – luminance (emitted light of the screen), in cd/m²

 $E_{v_{screen}}$ – illuminance (incident light to the screen), in lux

 G_{screen} – screen gain

Screen gain in multi-planar volumetric screen is based on the scattering quality of the optical shutters. Actual numbers for screen gain are not available publicly thus, screen gain of '1' will be used with additional angular distribution. Liquid crystal shutter scattering state angular distribution is explained in [56] and *Park G., et al* [57, Fig. 4] reports that the distribution form is similar to cosine function:

$$G_{\text{screen}} = 1 \cdot \cos(\varphi_{\text{obs}}) \tag{4.15}$$

where φ_{obs} – angle of observation (0° is perpendicular to the screen).

Illuminance is the total luminous flux incident on a surface, per unit area and can be calculated by dividing luminous flux reaching the screen by the screen size as shown in the equation:

$$E_{\mathbf{v}_{\text{screen}}} = \frac{\phi_{\mathbf{v}_{\text{screen}}}}{d_{\mathbf{w}} \cdot d_{\mathbf{h}}} \tag{4.16}$$

where $\phi_{v_{screen}}$ – luminous flux in lm;

 $d_{\rm w}$ – screen horizontal size in m;

 $d_{\rm h}$ – screen vertical size in m.

Luminous flux is the luminous energy per second (light) that reaches the screen. Light originates from solid state light sources and is attenuated by an optical light path, a relay system as well as time based modulation and shutter transient effects. Mathematically it is expressed as:

$$\phi_{v_{\text{screen}}} = \phi_{v_{\text{source}}} \eta_{\text{passiveElements}} \eta_{\text{slm}}(t) \eta_{\text{vs}} \eta_{\text{vst}}(t)$$
(4.17)
Ix radiated by light source in lm:

where $\phi_{v_{source}}$ – luminous flux radiated by light source in lm;

 $\eta_{\text{passiveElements}}$ – transmittance of optical system passive components (mirrors, lenses, ...);

 $\eta_{\rm slm}(t)$ – time based transmittance of spatial light modulator;

 η_{vs} – transmittance of volumetric screen optical properties;

 $\eta_{\rm vst}(t)$ – transmittance of volumetric screen time based properties.

Spatial light modulator relative time based attenuation is governed by SLM input parameters: binary pattern rate and mirror reset time and is expressed as light amount over time period (based on modulation method) relative to maximal achievable light amount over the same time period (also based on modulation method). This is shown in Eq. (4.18).

$$\eta_{\rm slm}(t) = \frac{\phi_{\rm avg}(\rm mode)}{\phi_{\rm avg}(\rm max)}$$
(4.18)

Average luminous flux over given time period can be expressed as integral:

Modulation method

Method (short)	$N_{\mathbf{b_{pwm}}}$	$N_{\mathbf{b}_{\mathrm{lsim}}}$
Binary pulse-width (PWM)	$\neq 0$	= 0
Light source intensity (LSIM)	= 0	$\neq 0$
Mixed (mixed)	$\neq 0$	$\neq 0$

$$\phi_{\text{avg}}(t) = \frac{1}{t_{\text{per}}} \int_0^{t_{\text{per}}} \phi(t) dt$$
(4.19)

where ϕ_{avg} – average luminous flux in the given time period;

 $t_{\rm per}$ – given time period for calculating luminous flux;

 $\phi(t)$ – function representing luminous flux waveform in the given period.

The chosen modulation method is mathematically represented by two parameters: N_{bpwm} and N_{blsim} (shown in Table 4.1). If a pixel's intensity is defined as a *N*-bit integer, then each bit from $[0 \dots (N - 1)]$ must be output with binary radix weighted values of luminous energy. This means that if (*i*)'th bit luminous energy is Q_v , then (*i* + 1)'th bit luminous energy shall be $2 Q_v$.

The pulse-width modulation timing diagram is depicted in Fig. 4.1. Overall luminous energy per period $t_{perPwmBits}$ is divided by binary-weighted time steps. Smallest step t_{pwmBit} represents time period during which least significant bit representing bitplane is visible on SLM surface. Next more significant bit time step is binary (two) times longer $t_{pwmBit}(LSB + 1) = 2 t_{pwmBit}(LSB)$.

Assuming a constant light source luminous flux $\phi_{v_{source}} (N_{b_{pwm}} \neq 0; N_{b_{lsim}} = 0) = \text{const}$, pulsewidth light intensity modulation average luminous flux for given time period $t_{perPwmBits}$ (defined by Eq. (4.8)) can be calculated by Eq. (4.19) and in a simpler form by Eq. (4.20). The equation shows that the average luminous flux is not dependent on SLM timing parameters or the number of bits to be modulated in PWM modulation mode.



Figure 4.1: Pulse width modulation bit luminous energy relation diagram.

$$\phi_{avg} \left(N_{b_{pwm}} \neq 0; N_{b_{lsim}} = 0 \right) = \phi_{v_{source}}$$
(4.20)
relative luminous flux (constant for DWM mode, value of 100 % or 1)

where $\phi_{v_{source}}$ – light source relative luminous flux (constant for PWM mode, value of 100 % or 1).

Light source intensity modulation is depicted in Fig. 4.2. LSIM mode requires constant time steps for each bitplane (t_{lsimBit}) and luminous energy is adjusted by changing the light source intensity (binary weighted). For example, assume luminous energy for *i*'th bit of $Q_v = t_{\text{lsimBit}} \phi_{v_{\text{source}}}$, next (*i* – 1)'th bit luminous energy is expressed as $\frac{1}{2}Q_v = \frac{1}{2}(t_{\text{lsimBit}}\phi_{v_{\text{source}}})$ and by LSIM definition $t_{\text{lsimBit}} = \text{const}$, then $\frac{1}{2}Q_v = t_{\text{lsimBit}}\frac{1}{2}\phi_{v_{\text{source}}}$.



Figure 4.2: Light source intensity modulation bit luminous energy relation diagram.

Luminous flux of *i*'th bit $(0 \le i \le N - 1)$ can be be calculated by Eq. (4.21). Assuming that the most significant bit (N - 1) luminous flux is set to maximum relative light source value $(\phi_{v_{source}}(N - 1) = 1)$, Eq. (4.21) can be simplified to Eq. (4.22).

$$\phi_{v_{\text{source}}}(i) = \frac{1}{2^{((N-1)-i)}} \phi_{v_{\text{source}}}(N-1)$$
(4.21)

$$\phi_{\mathbf{v}_{\text{source}}}(i) = \frac{1}{2^{((N-1)-i)}}$$
(4.22)

The LSIM depiction in Fig. 4.2 shows that the overall period average luminous flux can be calculated by summing each bit representing luminous flux values (Eq. (4.22)) and dividing by the number of bits:

$$\phi_{\text{avg}} \left(N_{\text{b}_{\text{pwm}}} = 0; N_{\text{b}_{\text{lsim}}} \neq 0 \right) = \frac{1}{N_{\text{b}_{\text{lsim}}}} \sum_{i=0}^{N_{\text{b}_{\text{lsim}}}-1} \frac{1}{2^{\left((N_{\text{b}_{\text{lsim}}}-1)-i \right)}}$$
(4.23)

where $N_{b_{lsim}}$ – light source intensity modulated bits.

The equation shows that for any integer number $N_{b_{LSIM}} > 1$, luminous flux is $\phi_{avg}(LSIM) < 1$. This means that Eq. (4.18) reference max value is $\phi_{avg}(PWM)$.

Mixed modulation is depicted in Fig. 4.3. The figure shows that $N_{b_{lsim}}$ bits are modulated with LSIM (luminous flux values changes) and $N_{b_{pwm}}$ bits are modulated with PWM (time step duration changes). Fig. 4.4 shows the bit notation used in expressions that characterizes bit distribution of mixed modulation mode.

PWM and LSIM bit periods t_{lsimBit} and t_{pwmBit} are not strictly obliged to be equal. For the correct mixed modulation mode LSIM part calculation, the most significant LSIM bit luminous flux value must be expressed in terms of time periods and luminous flux of PWM bits. Most significant LSIM bit luminous energy shall be $\frac{1}{2}$ of the least significant PWM bit luminous energy, as shown here:

$$Q_{\rm v}({\rm MSB},{\rm LSIM}) = \frac{1}{2}Q_{\rm v}({\rm LSB},{\rm PWM})$$

Luminous energy can be expressed as luminous flux and time period multiplication using a geometrical approach thus, rewriting the previous equation as:



Figure 4.3: Mixed intensity modulation bit luminous energy relation diagram, $N_{b_{pwm}} = 3$, $N_{b_{lsim}} = 3$, $t_{lsimBit} = t_{pwmBit}$.



Figure 4.4: Mathematical notation of mixed modulation mode bit descriptions.

$$\phi_{v_{source}}(MSB, LSIM) t_{lsimBit} = \frac{1}{2} \phi_{v_{source}}(LSB, PWM) t_{pwmBit}$$

Solving expression for $\phi_{v_{source}}(MSB, LSIM)$ results in Eq. (4.24).

$$\phi_{\mathbf{v}_{\text{source}}}(\mathbf{MSB}, \mathbf{LSIM}) = \frac{1}{2} \frac{t_{pwmBit}}{t_{lsimBit}} \phi_{\mathbf{v}_{\text{source}}}(\mathbf{LSB}, \mathbf{PWM})$$
(4.24)

Previously calculated timing values for bit period lengths (Eq. (4.10) and Eq. (4.11)) can be inserted in Eq. (4.24) and results in the coefficients shown in Eq. (4.25) for *DLP7000* SLM unit.

$$\phi_{v_{\text{source}}}(\text{MSB}, \text{LSIM}) = \\ = \phi_{v_{\text{source}}}(\text{LSB}, \text{PWM}) \frac{1}{2} \begin{cases} 0.71 & \text{PWM with phased pat. mode} \\ 1 & \text{PWM with global pat. mode} \end{cases}$$
(4.25)

It is now possible to construct average luminous flux calculation for the mixed modulation mode. The mathematical expression consists of two main parts: the average luminous flux for LSIM bit modulation and the average luminous flux for PWM bit modulation in the following form:

$$\phi_{\text{avg}}(N_{\text{b}_{\text{pwm}}}, N_{\text{b}_{\text{lsim}}}) = \frac{Q_{\text{pwm}} + Q_{\text{lsim}}}{t_{\text{perPwmBits}} + t_{\text{perlsimBits}}}$$
(4.26)

Luminous energy for PWM bits can be calculated by inserting Eq. (4.20) in Eq. (4.26):

 $Q_{\text{pwm}} = t_{\text{perPwmBits}} \phi_{\text{avg}} \left(N_{\text{b}_{\text{pwm}}} \neq 0; N_{\text{b}_{\text{lsim}}} = 0 \right)$ (4.27) where Q_{pwm} – Luminous energy during PWM bits.

Luminous energy for LSIM bits can be calculated by a combination of Eq. (4.21) and Eq. (4.24). The series shown in Eq. (4.23) must be rewritten slightly to accommodate the fact that the most significant LSIM bit is not output with a luminous flux of 100 % as if it were in the pure LSIM mode but rather with luminous flux representing $\frac{1}{2}$ of the least significant PWM bit luminous energy.

The coefficient $\frac{1}{2}$ from Eq. (4.24) is included in Eq. (4.28) by changing the starting sum index from 0 to 1, as $\frac{1}{2^1} = 0.5$ as required. The timing coefficient $\frac{t_{pwmBit}}{t_{lsimBit}}$ is included as a multiplier to cover the possibility of different pattern output lengths.

$$Q_{\rm lsim} = t_{\rm perLsimBits} \frac{t_{\rm pwmBit}}{t_{\rm lsimBit}} \frac{1}{N_{\rm b_{\rm lsim}}} \sum_{i=1}^{N_{\rm b_{\rm lsim}}-1} \frac{1}{2^i}$$
(4.28)

where Q_{lsim} – Luminous energy during LSIM bits.

Combining the PWM part (Eq. (4.27)) and the LSIM part (Eq. (4.28)) in Eq. (4.26) and results in:

$$\phi_{\text{avg}} \left(N_{\text{b}_{\text{pwm}}} \neq 0; N_{\text{b}_{\text{lsim}}} \neq 0 \right) =$$

$$= \frac{t_{\text{perPwmBits}} \phi_{\text{avg}} \left(N_{\text{b}_{\text{pwm}}} \neq 0; N_{\text{b}_{\text{lsim}}} = 0 \right)}{\left(t_{\text{perPwmBits}} + t_{\text{perLsimBits}} \right)} + \frac{t_{\text{perLsimBits}} \frac{t_{\text{pwmBit}}}{t_{\text{lsimBit}}} \frac{1}{N_{\text{b}_{\text{lsim}}}} \sum_{i=1}^{N_{\text{b}_{\text{lsim}}}-1} \frac{1}{2^{i}}}{\left(t_{\text{perPwmBits}} + t_{\text{perLsimBits}} \right)}$$

$$(4.29)$$

The equation (4.29) represents the average luminous flux calculation for mixed modulation method. The summary of the three modulation methods' optical transmittance is shown in the formula:

$$\eta_{\rm slm}(\rm mode) = \frac{1}{\phi_{\rm avg}(PWM)} \cdot \begin{cases} \phi_{\rm avg}(PWM) & \text{for } PWM \\ \frac{1}{N_{\rm b_{lsim}}} \sum_{i=0}^{N_{\rm b_{lsim}}-1} \frac{1}{2^{i}} & \text{for } LSIM \\ \frac{Q_{\rm pwm}+Q_{\rm lsim}}{(t_{\rm perPwmBits}+t_{\rm perLsimBits})} & \text{for mixed} \end{cases}$$
(4.30)

The next variable in Eq. (4.17) is the volumetric screen light transmittance, which is based on the number of shutters and each shutter transmittance as shown in Eq. (4.31).

$$\eta_{\rm vs} = \eta_{\rm open}^{N_{\rm layers}} \tag{4.31}$$

where η_{open} – open state transmittance of a single optical shutter;

 N_{layers} – number of optical shutters.

Volumetric screen switching light transmittance is an optical parameter that shows light loss over the period of a whole volumetric image projection. This parameter can be calculated as a proportion between total active image time and total volumetric image time (including dead time during shutter switching) and can be expressed in the formula as:

$$\eta_{\rm vst} = \frac{t_{\rm active}}{t_{\rm active} + t_{\rm depthBlanking} + t_{\rm layerBlanking}} \tag{4.32}$$

4.3 Color Depth

Color depth is a parameter that characterizes the number of different colors a visualization system can produce. The number of color variations depends on the number of colors and bits per single color as shown in Eq. (4.33).

$$N_{\text{colVars}} = 2^{(N_{\text{bpc}} N_{\text{colors}})} = 2^{\left((N_{\text{bpwm}} + N_{\text{b}_{\text{lsim}}}) N_{\text{colors}}\right)}$$
(4.33)

 $N_{\text{colVars}} = 2^{(N_{\text{bpc}}, N_{\text{colors}})} = 2 \sum_{i=1}^{N_{\text{colVars}}} N_{\text{colVars}}$ where N_{colVars} – total number of possible color variations;

 $N_{b_{nwm}}$ – number of pwm modulated bits;

 $N_{b_{lsim}}$ – number of lsim modulated bits;

 $N_{\rm colors}$ – number of base colors.

4.4 3D Quality Parameters

4.4.1 Volume Resolution and Density

Volume resolution or the total number of voxels is a product of horizontal, vertical, and depth resolution. The number of horizontal and vertical pixels is given by the spatial light modulator input parameters $N_{\rm w}$ and $N_{\rm h}$. Depth resolution is given by the number of depth planes variable $N_{\rm layers}$ and the calculation is shown in Eq. (4.34). Volume pixel density is a parameter that characterizes the number of voxels per volume (how dense is the volume). It can be calculated by dividing the number of voxels with the volume size in cm³ (Eq. (4.35)).

$$N_{\rm volRes} = N_{\rm w} \, N_{\rm h} \, N_{\rm layers} \tag{4.34}$$

where N_{volRes} – total number of voxels.

$$N_{\rm volDens} = \frac{N_{\rm volRes}}{d_{\rm w} d_{\rm h} d_{\rm layers} \left(N_{\rm layers} - 1\right)}$$
(4.35)

where N_{volDens} – volumetric density;

 $d_{\rm w}$ – optical shutter horizontal size;

 $d_{\rm h}$ – optical shutter vertical size;

 d_{lavers} – distance between two sequential depth layers.

4.4.2 3D Perception Score

The introduction of the 3D perception metric for a volumetric display can be based on a similar issue for 2D images, meaning the perception of the depth based on the image resolution. *Tsushima Y*, *et al* [58] analyzes how resolution of a 2D image impacts depth perception and argues that higher resolution of a 2D image increases depth perception of a shaded image, while much stronger depth indicators are motion parallax and binocular disparity. They report a logarithmic relation between perception and resolution as shown in [58, Fig. 3]. *Masaoka K., et al* [59] comes to a similar conclusion, showing a logarithmic relation between resolution and sensation of realness in [59, Fig. 12]. *Nur, G. et al* [60] reports a similar effect while researching the impact of the depth map spatial resolution impact on 3D video quality. The perceived effect gradually increases until a certain threshold is reached. The authors characterize depth perception using words such as "*Bradley-Terry Score*" and "*Sensation of Realness*" and for 3D perception the term "*Score*" will be used.

These references agree on logarithmic type of relation between resolution and depth perception. Similar theory could be used in multi-planar volumetric display technology. The 3D perception score increases as a logarithmic function of the depth resolution N_{layers} as shown in Eq. (4.36). Moreover, according to *Sullivan A*. [61], the perceivable depth plane number can be increased by applying antialiasing techniques creating apparent voxels between two sequential depth planes.

$$N_{\text{score3D}} = \log_{10}(N_{\text{layers}}) \tag{4.36}$$

where N_{score3D} – 3D perception characteristic parameter "Score".

This theory is tested by using the user evaluation experiment with the implemented device and the results are discussed in Sec. 6.4

5 Model Analysis and Local Parameter Optimization

Visualization system model analysis is a summarizing chapter that joins together previous chapters: input parameters and the system model. The analysis process, results and conclusions are based on various input parameter impact to the visualization system. This chapter is divided into the following parts: an introduction to analysis process, followed by the impact determination of various input parameters and their groups and finished by conclusions.

The introduced system model can be represented as a black box with a number of inputs and outputs. Analysis and simulations can be carried out using various techniques such as MATLAB, Python, C# code, or implementing an application with a graphical user interface.

5.1 Introduction to Analysis Process

This system's model analysis and local parameter optimization attempt to find good input parameter sets that maximize an output parameter by keeping other output parameters within defined bounds.

In order to avoid computational issues, input parameters are grouped to isolate parameter impact. Partial analysis of specific parameters are carried out with other parameters kept at default values.

5.2 Partial Analysis of Input Parameters and Groups

5.2.1 Optical Shutter

Optical shutter input parameters are used to calculate refresh rate (t_{decay} , t_{rise}) and luminance (η_{open} , t_{decay} , t_{rise}).

Firstly, single shutter transient parameters' impact is analyzed by sweeping t_{decay} or t_{rise} values. Impact of transient parameters is also dependant on the chosen R_{db} and R_{dbs} input parameters thus, these parameters are also changed during analysis. The shutter switching impact result for no blanking $(R_{db} = 0)$ and full blanking $(R_{db} = 1)$ configuration is depicted in Fig. 5.1. The figure shows that if no blanking configuration is used, then there is no impact from shutter transient parameters. In the case of full blanking configuration, an impact with linear characteristics is observed. Considering shutters with transient response of 500 µs to 1000 µs, the relative refresh rate difference is from 0.79 to 0.65 or ≈ 20 %. A similar impact of the transient input parameters to the luminance is also observed.



Figure 5.1: Single shutter transient response refresh rate (also luminance) impact over sweep of t_{rise} .

The shutter's optical parameter impact to luminance is analyzed secondly by sweeping η_{open} . This results in relative luminance change as depicted in Fig. 5.2 and shows exponential relation to overall system luminance.



Figure 5.2: Single shutter brightness impact.



Figure 5.3: System relative refresh rate for various SLM.

Analysis shows that optical shutters should be chosen with the highest optical transmittance and lowest transient delay (this parameter is more important, since it impacts two output parameters – luminance and refresh rate).

5.2.2 Spatial Light Modulator

SLM parameters influence refresh rate and luminance. Figure 5.3 depicts relative refresh rate for available SLMs from *Texas Instruments*, sorted in ascending order. The figure shows *DLP7000* to be the most suitable due to the fact that it offers a ≈ 30 % increase in refresh rate over next SLM – *DLP9500*.

SLM mirror settling and reset time t_{slmRst} influence both refresh rate and luminance in a linear fashion as shown in Fig. 5.4. The impact to refresh rate is greater if the projection system configuration parameter $E_{PwmSlmGlobalRst}$ is set to 1, since with the flag, PWM modulated bits are output with the SLM global reset mode, which reduces overall frame rate. No impact to luminance is observed if $E_{PwmSlmGlobalRst}$ is set to 1.

Although analysis shows that mirror reset and settling time impact on refresh rate (shown in figure) is stronger than the impact on relative luminance in both cases the lower the mirror settling time, the better. SLM should be chosen with the highest refresh rate capability and the lowest mirror reset and settling time.

5.2.3 Light Source and Passive Elements

A light source luminous flux parameter is used to calculate the actual luminance value of the visualization system. Results of luminous flux sweep is depicted in Fig. 5.5. The graph shows that luminous flux impact is linear – the bigger the luminous flux value, the bigger the luminance value.

5.2.4 Multi-Planar Screen

Multi-planar screen characterizing input parameters impact most of the output parameters – refresh rate, luminance and 3D quality parameters. Figure 5.6 summarizes the relative impact of the number of shutters input parameter to refresh rate, luminance and 3D perception score.

The shape of both refresh rate and luminance impact function is reciprocal $\left(\frac{1}{x}\right)$, with slightly



Figure 5.4: SLM mirror reset and settling period impact to refresh rate.



Figure 5.5: Light source luminous flux impact on luminance.

different curves. For the default set of other input parameters, both curves overlap at $N_{\text{layers}} = 15$.

Furthermore, the number of shutters impact 3D perception quality (volume resolution, density and perception score). The proposed 3D perception score theory result is depicted in the figure as N_{score3D} line. The figure shows a logarithmic relation (adjusted from relative 0 to 1 for 5 to 50 shutters). From the observer point of view, the 3D score should be as high as possible even though it actually lowers available refresh rates and luminance levels. The proposed score should be adjusted and the minimum score for volumetric 3D usability should be introduced. The user evaluation test (explained in further sections) attempts to verify the proposed theory and introduce a minimum score for 3D perception.



Figure 5.6: Number of shutter impact to refresh rate, luminance and 3D perception score.

5.2.5 Modulation Method and Timing Analysis

Modulation method is defined by a relation of two input parameters – pixel grayscale binary bits modulated with PWM ($N_{b_{pwm}}$) and LSIM ($N_{b_{lsim}}$) as shown in Table 4.1. Analysis is carried out by setting other input parameters to the default values and analysing various combinations of $N_{b_{pwm}}$ and $N_{b_{lsim}}$, acquiring the resulting data sets.

Luminance as a function of $N_{b_{pwm}}$ and $N_{b_{lsim}}$ is depicted as a surface plot in Fig. 5.7(a). The figure shows that luminance value increases with higher PWM bit number value.



Figure 5.7: Relative luminance plot for various PWM and LSIM modulation bit values.

The modulation method influences the system in a non-linear manner. A local optimum of the two corresponding output parameters, meaning refresh rate and luminance, can be calculated by applying minimum constraint to refresh rate and analyzing luminance values. This is done by applying the minimum value ($R_{\rm fps}(\min) = 50$) refresh rate filter to luminance value results thus, filtering out all unacceptable results due to too low refresh rate. A minimum filter value of 25 Hz is also analyzed since volumetric image can be output on a multi-planar screen using an interlacing technique (one cycle produces all even slices, the second cycle produces all odd slices) resulting in flicker-free perception of the volumetric image.

The resulting surface plot for 50 Hz filtered results is shown in the Fig. 5.7(b). As shown in the figure, several points have been zeroed. As results are analyzed in the context of specific color depth $(N_{b_{pwm}} + N_{b_{lsim}})$ and to get results in the required format, the surface data plot is sliced diagonally and an example of the extracted slices is depicted in Fig. 5.8.

The horizontal axis shows possible modulation bit combinations that produce the color depth. Relative luminance is plotted in the vertical axis. Marked dots (the diamond marker) on the lines show valid luminance results after applying a minimum refresh rate filter. Note that PWM mode is plotted on the most left side of the figure ($N_{b_{pwm}}$, 0) and the LSIM mode is on the most right side of the figure (0, $N_{b_{lsim}}$). The figure shows that although the required minimum 50 Hz refresh rate is achieved by the LSIM mode with a relative luminance value of 0.28, the usage of mixed modulation method results in a higher relative luminance (in this case, value around 0.49), unless the refresh rate is achieved by PWM.



Figure 5.8: Relative luminance plot for 18 bits per pixel PWM and LSIM modulation bit combinations.

For a given color depth, the modulation method should be chosen to maximize the relative luminance by choosing the most leftwards valid (indicated by the diamond marker) modulation bit combination point on the plot. The mixed modulation method allows to achieve higher luminance values than LSIM for color depth where PWM does not achieve a minimum refresh rate.

Table 5.1

እ <i>T</i> * 1	1 1	•	1. 1.	•	· · ·	1 1 /	C 70	\ T T	105	TT C1/ 1	1
N/IVOC	modulation	$\alpha_{01} n \alpha_{11}$	or light	cource in	toneity	modulation	tor N	1 117	and is	H7 TITAPAN	V011100
IVIIACU	modulation	2 and OV	сі пеш	source m	ICHSILV.	modulation	101.3		and ΔJ	IIZ IIIUIUU	values.
		· · ·									

color depth		50	Hz fps			25	25 Hz fps		
(bits)	PWM	LSIM	mixed (p,l)	gain	PWM	LSIM	mixed (p,l)	gain	
8	_	_	0.18 (1,7)	_	_	0.25	0.77 (4,4)	209 %	
7	_	0.28	0.39 (2,5)	38 %	_	0.28	0.81 (4,3)	189 %	
6	_	0.33	0.44 (2,4)	36 %	_	0.33	0.87 (4,2)	165 %	
5	_	0.38	0.76 (2,3)	97 %	_	0.38	0.91 (4,1)	136 %	
4	_	0.47	0.83 (3,1)	77 %	1	0.47	0.83 (3,1)	0 %	
3	1	0.58	0.68 (2,1)	0 %	1	0.58	0.68 (2,1)	0 %	

Results are shown in Table 5.1. Assuming 50 Hz filtered results and color depth of three to eight bits, the usage of the mixed modulation mode increases relative luminance by 38 % to 97 %, where applicable. A similar approach can be used for different minimum value filters. For 25 Hz filtered results and color depth of three to eight bits, mixed modulation mode increases luminance from 136 % to 209 %, where applicable.

Additional input timing parameters that influence the system are blanking periods R_{db} and R_{dbs} . The impact of inter-layer blanking period (controlled by R_{db}) insertion is depicted in Figure 5.9. The figure shows that the impact is linear and the strength (slope) is dependent on the shutter transient response. In other words, how fast it can switch. Impact of R_{dbs} is not depicted separately being similar to Fig. 5.9 but with less weight.



Figure 5.9: Inter-layer blanking period impact on refresh rate for various shutter transient response times.

5.3 Summary and Conclusions

Nonconfigurable parameters

Parameters in this group impact the visualization system model in a linear fashion. The minimum or maximum of resulting output parameters are located at the minimum or maximum of input parameter. In choosing the system's element implementation, it should be done with the best available shutter, the fastest available SLM and the strongest light source. It is important to choose elements that support minimum output parameter values.

Configurable parameters

Configurable parameters impact the model output parameters in both a linear and non-linear way. The choice of the modulation method and timing parameters can be configured during the operation of the system but multi-planar screen parameters have to be decided before developing the experimental device. To test the 3D perception quality theory, a prototype device will be created with a 20 layer deep multi-planar screen.

6 Experimental Device Implementation

This chapter describes the real visualization system implementation in FPGA hardware based on the system modelling and analysis mentioned previously, in chapters 2–5. The system's basic architecture building blocks are shown in Fig. 2.2 and this chapter will explain implementation of the volumetric image data transfer and implementation of the whole 3D visualization system.

6.1 Volumetric Data Transfer

Volumetric data transfer implementation is required to transfer a 3D image scene from the source to the visualization system. The visualization system requires a real time data transfer. An overview of the proposed data transfer system is shown in Fig. 6.1. An image source is defined as a three dimensional matrix of pixel data located in computer RAM memory (volumetric image generation or acquisition, pre-processing, and rendering are done beforehand, and are beyond the scope of this thesis).

6.1.1 Characteristics of Volumetric Video Stream

Volumetric 3D image consists of three spatial dimensions (height, width and depth) and resolution is defined as $x \times y \times z$, for example, $1024 \times 768 \times 20$ for 1024 horizontal pixels, 768 vertical pixels and 20 depth pixels, resulting in 15.7 million volumetric pixels (or voxels).

The size of a single volumetric image (in bits) can be calculated by multiplying the numbers of volumetric resolution by color depth (bits per voxel) as shown in Eq. (6.1).

$$N_{\rm size} = N_{\rm w} N_{\rm h} N_{\rm layers} N_{\rm bpc} N_{\rm colors} \tag{6.1}$$

where N_{size} – binary size of a single volumetric image for given resolution and color depth.

For $(1024 \times 768 \times 20)$ resolution, 24 bits per pixel (8 bits per color), a single volumetric image size is 377,487,360 bits (45 MiB). In order to achieve a real time volumetric 3D video stream, it is required to transfer these volumetric images to the volumetric display at a sufficient update rate (frames per second) and the required data bandwidth can be calculated by Eq. (6.2). To transfer 25 frames per second with the previous resolution and color depth the required data bandwidth is 9,437 Mb/s. This is the minimum required video data transfer bandwidth that must be supported by each data transmission system interface layer.

$$N_{\rm bw} = N_{\rm size} R_{\rm fps} \tag{6.2}$$

where $N_{\rm bw}$ – required bandwidth for 3D image transfer, bits per second;

 $R_{\rm fps}$ – image update rate, frames per second (FPS).

6.1.2 Software Level Data Transfer

Due to bandwidth and flexibility (analyzed in the thesis), *Peripheral Component Interconnection express* (PCIe) is chosen as the basis of software to hardware data transfer layer implementation. PCIe is a layered standard that consists of a user interface layer, a transaction layer, a data link layer and



Figure 6.1: Data transfer layer structure.

a physical layer. Required functionality can be implemented in the FPGA chip and FPGA vendors offer solutions for PCIe layer implementation (soft or hard IP Cores) and was carried out using *Xilinx Virtex-6* FPGA.

Each single PCIe data lane is connected to FPGA transceiver and *Xilinx* Hard-IP core block called "PCIe Endblock". Xilinx offers a reference design for PCIe LogiCORE IP [62], which is compliant with the PCI Express Base Specification Rev 2.0. It supports both the Gen1 and Gen2 PCIe connection. The top level IP Core functional block incorporates multi gigabit transceivers and Integrated PCIe Block.

Xilinx LogiCORE IP Core is first generated and configured for PCIe *Gen2*. This core is interfaced by a custom designed user interface layer module, which implements a direct memory access end point. In this module, the video data is extracted from packets and is put in a first-in, first-out (FIFO) buffer for use in the DDR3 memory controller. Architecture of such PCIe controller is shown in Fig. 6.2.



Figure 6.2: Xilinx FPGA based PCIe controller architecture.

PCIe implementation at an operational system level is as follows: firstly, the PCIe card is enumerated in BIOS; secondly, a specific part of RAM common-buffer is used to store data for PCIe DMA transfers.

Custom *Windows* and *Linux* PCIe drivers are used to interface the FPGA, with similar supported data rates in both operational systems. Prepared video data are loaded to the RAM common buffer by the software driver (the hard disk drive is not used thus, speeding up the process).

Effective measured DMA based data bandwidth is around 56 % of the rated PCIe transfer rate. Bandwidth is reduced by: *8b/10b* physical encoding (80 %), TLP header/data ratio (86 %), DMA management (80 %), resulting in 11.2 Gb/s bandwidth that allows for a 3D volumetric image transfer rate of 30 Hz. The benchmark was measured on a personal computer with the following parameters – *Asus P8Z68-V PRO/GEN3* motherboard, *Intel Core i5-2400* CPU, 8 GB 1.3 GHz DDR3 RAM, *Xilinx ML605* development board plugged in PCIe socket, *Intel SSD* 60 GB HDD, *Windows* 7 and *Linux openSUSE 12.1* operational systems.

6.1.3 Hardware Level Data Transfer

The next step of volumetric image stream implementation is creating an inter-device data link. This means a hardware data transfer between the computer system's PCIe card and the volumetric 3D visualization system. The volumetric 3D image stream is a completely new requirement for video standards and none of them support such standard out of the box.

Video transfer standard analysis shows that standards with the most bandwidth are *HDMI* and *DisplayPort*. A comparison of *HDMI 1.4* and *DisplayPort 1.2* (*DP*) is presented in this thesis and it shows that *DisplayPort* is better suited for the required application due to the following reasons:

- DisplayPort 1.2 offers the highest bandwidth with raw data transfer speed of 21.6 Gbit/s [63];
- It is based on a flexible micropacket data transfer [64];
- It supports custom display resolutions;
- Configurable timing parameters (length of blanking periods, front porch, sync pulse, back porch, etc.) allow to increase the effective data transfer rate.

6.1.3.1 Volumetric 3D image stream mapping on DisplayPort

It is required that volumetric 3D image transfer sends information that defines the current depth plane. Such an option is possible with the following solutions:

- Each depth plane is transferred as a separate image stream using *DP 1.2 Multi Stream Transfer* feature. In this case, up to 63 depth planes are addressable.
- Each depth plane is sent sequentially and the currently transferred depth plane identification number is sent using Extension Packet, before each frame;
- Depth planes are stacked within a higher resolution 2D image, such as custom resolution of 4095 x 3840 pixels.

Implementation of the experimental device requires addressing of 20 depth planes. This is executed by the second option. The volumetric 3D video depth images are transferred sequentially as shown in Fig. 6.3. The figure shows transfer of two depth layers, each with y number of rows.



Figure 6.3: 3D image row, column and depth timing scheme.

Classically long blanking periods (used for cathod ray return) are not required since image transfer is asynchronous to the projection system and *DisplayPort* supports the shortest blanking periods of five clock cycles for horizontal and 17 for vertical. The addition of extension packet extends VBP to 26 cycles. The minimum length of VBP contents are depicted in Fig. 6.4. The extension packet is configured to contain current depth and total depth values.



Figure 6.4: Vertical blanking period (26 cycles).

Volumetric image transfer rate per second can be calculated by combining available *DisplayPort* data rate and bandwidth used for blanking periods. The *DisplayPort 1.2* available data bandwidth is defined as shown in Eq. (6.3).

 $N_{bw_{DP}} = f_{sym} N_{lanes} N_{bits_{DP}} = 540 \cdot 10^{6} \cdot 4 \cdot 8 = 17.28 \, Gb/s \tag{6.3}$ where $N_{bw_{DP}} - DisplayPort 1.2$ available data bandwidth; $f_{sym} - DisplayPort 1.2$ symbol clock (540 MHz); $N_{lanes} - DisplayPort 1.2$ data lanes; $N_{bits_{DP}} - bits$ per lane, per symbol clock cycle (after deserializer).

By knowing the length of the horizontal and vertical blanking periods, the maximum volumetric image $(1024 \times 768 \times 20 \text{ resolution and } 24 \text{ bits per pixel})$ transfer rate using *DisplayPort 1.2* is calculated by Eq. (6.4).

$$R_{\rm fps_{\rm DP}} = \frac{N_{\rm bw_{\rm DP}}}{N_{\rm size}} \frac{N_{\rm w} N_{\rm h} \frac{N_{\rm colors}}{N_{\rm lanes}}}{N_{\rm w} N_{\rm h} \frac{N_{\rm colors}}{N_{\rm lanes}} + N_{\rm blanking}} = 45.42 \, fps \tag{6.4}$$

where $\frac{N_{\text{colors}}}{N_{\text{lanes}}}$ – *DisplayPort* coefficient (4 RGB pixels in 3 clock cycles); N_{blanking} – total number of blanking period symbols per frame.

6.1.3.2 Experimental setup

The main purpose for the experimental test system is to implement the high speed data link between two devices based on *DisplayPort 1.2* and volumetric image mapping. Implementation, testing and verification setup consist of the following parts – *DisplayPort* transmitter (TX) design in FPGA, *DisplayPort* receiver (RX) design in FPGA and multiple board-to-board hardware connections (such as close-loop, single channel configuration, and full four channel configuration).

Two *Xilinx ML605* development kits [65] with *FMC XM104* daughter boards [66] are used for the test system development. These tools allow for different clock rates and multiple lane connection experiments.

Single lane test system

The single lane *DisplayPort 1.2* test system is created by using a physical loopback with 2x *SMA* connections on a single ML605 development board. This configuration lets one verify the *DisplayPort* standard concept usability for 3D imaging applications.

The *DisplayPort 1.2* compatible volumetric 3D image source generator is developed and synthesized in VHDL. Module generates the required number of pixels and rows and depth planes and inserts HBPs and VBPs packets into the data lane.

FPGA transceivers (both TX and RX) are configured to implement *8b/10b* encoder (*10b/8b* for RX) and data serialization of 20x (deserialization for RX). The system clock is 156.25 MHz and for this test, transceivers are configured to 3.125 Gbit/s.

The test system configuration successfully verified the application of *DisplayPort* using the integrated *ChipScope Logic Analyzer*. The results show that volumetric images can be successfully extracted from a high speed serial data stream using transceivers and receiver logic.

Four lane test system

More sophisticated and complete verification is carried out by implementing all four *DisplayPort* channels. Such a test system's schematic is shown in Fig. 6.5. Two *ML605* development kits with *XM104 FMC* boards are connected via *CX4* cable (10 Gbit ethernet cable, four lanes, each running at 3.125 Gbps).

The transmitter (*ML605 "1"*) implements a 3D image source generator and a *DisplayPort* main link with full four lanes connected to their transceivers. The four transceivers are configured in TX only mode, the *8b/10b* buffer is enabled and data serialization is at the 20x input speed.

The receiver (*ML605"2"*) instantiates four transceivers in RX only mode with enabled serial-toparallel converter and the *10b/8b* buffer. Transceivers also provide clock recovery (recovers symbol clock) and channel bonding (removes *DisplayPort* inter-lane skew). This fulfills the *DisplayPort* physical layer functions. The *DisplayPort* sink is designed as receiver logic module that unpacks the main stream, extracts stream attributes and buffers data into the required order in a storage maintenance logic.

This experimental test setup was successfully analyzed and verified using the integrated *Chip-Scope Logic Analyzer* and forms a basis for a design choice to use *DisplayPort 1.2* as the data carrier in the final system.

DisplayPort integration with PCIe

Integration of PCIe and *DisplayPort* is done by decoupling with a frame buffer in DDR3 RAM. PCIe and *DisplayPort* run at different clock rates, and the frame buffer ensures complete asynchronous operation.

Data bus interface width from PCIe controller is 64 b, DDR3 controller - 256 b, DisplayPort - 64



Figure 6.5: *DisplayPort* four lane test configuration schematic.

b. Video pixel size is 24 bits and 32 pixels can be fit into 768 b wide register. 512 b and 256 b wide registers cannot hold an integer of pixels; thus, a 768 b register buffer is created for temporary storage of 32 pixels. Data is mapped from the registers to the *DisplayPort* data lanes as shown in Figure 6.6.



Figure 6.6: Video pixel mapping (R - red, G - green, B - blue, R0 - 0-th pixels red color, R31 - 31th pixels red color).

6.2 Implementation of Volumetric Visualization System

Volumetric 3D visualization consists of multiple electronic boards (drivers). The functionality of the electronics boards are:

- Main image processing board implements the controller, receives the volumetric data stream, drives the *Digital Light Processing* chipset, controls and synchronizes other modules;
- Multi-planar screen shutter driver board drives the liquid crystal shutters with a high voltage precise timing waveform;
- Light source driver board PWM and LSIM capable electronics system for driving high brightness LEDs.

This section focuses on the controller element that joins together various electronic modules: a volumetric 3D image stream, an SLM chipset driver, a multi-planar screen driver and a light source driver.

The key implemented features in the controller are as follows:

- Volumetric data path (critical signal path) *DisplayPort* reception, volumetric video data formatting, buffering, output to *Digital Light Processing* projection system;
- Control and synchronization of shutter screen driver and LED driver- data update, sync signals;

• Control path – control of whole volumetric display as a single system based on *MicroBlaze* soft processor;

Controller architecture with the corresponding module clock domains is shown in Fig. 6.7. Most of the FPGA components (IP cores) are custom designed, except for the modules in gray shading. The FPGA design is fully synchronous including the specifically designed and tuned reset procedure. The soft processor allows one to separately switch on/off different parts of the system.



Figure 6.7: Main board controller FPGA architecture with clock domains.

6.2.1 Critical signal path

The purpose of the critical signal path is passing the received volumetric image stream to the frame buffer (implemented as external DDR3 RAM) and the reading of the frame buffer when required by the DMD controller. Critical signal path implementation presents a challenge. This is because of multiple wide signal clock domain crossings and pipelined pixel-based data-stream mapping into the binary pattern-based data-stream. Critical signal path modules are as follows:

- *DisplayPort* clock domain *DisplayPort* physical receiver (*Xilinx GTX* transceivers), *DisplayPort* logic receiver (*DisplayPort receiver*) and pixel to bitplane mapper;
- DDR3 clock domain DDR3 memory driver;
- DMD controller clock domain DMD controller;

Clock domain crossing occurs at multiple places, as can be seen in Fig. 6.7. Data bus clock domain crossing is implemented by using *Xilinx Block RAM* based asynchronous FIFO buffers. Control, synchronization and informative signals (that are often in parallel with data buses), are passed using the single-double buffering method [67].

Xilinx GTX transceivers are configured to implement *DisplayPort* physical interface (four transceivers, each running at 3.125 Gbit/s or 5.4 Gbit/s), the *10b/8b* decoder, a 20:1 deserializer and channel bonding. The transceiver combined output data width is 64 b that is passed to the *DisplayPort* logic receiver module.

DisplayPort receiver module combined with *Pixel to Bitmap mapper* module:

- 1. Extracts data packets (image rows, HBP, VBP) and decodes image stream configuration data from VBP meaning resolution, current depth layer, number of depth layers, color depth to name a few;
- 2. Converts pixel-based data stream to binary pattern-based data stream by applying a three-level buffer stage and pipelined registers. Partial pixel to bitplane translation for single color (red) eight bits is shown in Fig. 6.8. The first four pixels are put in the corresponding buffer register bit locations (0, 1, 2, 3rd places) and each color bit is placed in a separate buffer register;

3. Assigns DDR3 memory mapped address (based on current row and depth layer).



Figure 6.8: Pixel to bitplane conversion.

6.2.2 Digital Light Processing interface controller

The DLP digital data interface is defined by the *DLPC410* chipset. The maximum data clock frequency is 400 MHz (dual data rate), the width is 32 b, resulting in a bandwidth of 25.6 Gbps. The interface is implemented in the *DMD Controller* module and the architecture is shown in Fig. 6.9. It is configurable and supports the modulation methods and data loading methods as discussed in Subsec. 2.3. An overview of the implemented algorithm is explained below:

- 1. System management issues the start command;
- 2. *DMD controller* samples and stores configuration values (modulation method, loading method, color depth and others) and starts the read address generator for the *DDR3 controller*;
- 3. Based on the chosen modulation method, binary patterns are read from FIFO and loaded to the DMD and reset at the necessary timing. Synchronization signals are sent to the shutter screen driver and LED driver board.

The highest verified volumetric refresh rate is around 77 Hz, which would correspond to 2D refresh rate of $20 \cdot 77 = 1540$ Hz.

6.2.3 Vizualization System Controller Management

The volumetric visualization system controller is management by a *Xilinx MicroBlaze MCS* soft processor. It resets and enables FPGA modules, sets parameters for modules and also implements various higher-level functions such as visual menu screen on the volumetric display, start-up screen, module start and stop sequences.

These functions and system statuses are also accessible from the computer through *USB-UART* connection and it allows a computer application to monitor and configure display statuses (temperatures, configuration register values, current modulation method, among others).





6.3 Demonstration Device

The designed and manufactured first unit of 3D volumetric display demonstrator is depicted in Fig. 6.10. This visualization system is put inside a 19" 14U transportation box, accompanied by a workstation for providing volumetric image data.



Figure 6.10: Demonstration device, courtesy of SIA Lightspace Technologies

6.4 User Evaluation and Experience Test

User evaluation is required to verify assumptions made in model mathematical analysis (Chapter 5) and is carried out using the *ITU Radiocommunication Sector* (*ITU-R*) recommendation (*ITU-R BT.500-13* [68]) for image quality subjective assessment methodologies. Choice of the assessment method is based on the "Selection of test methods" table found in the recommendation on page 10.



Figure 6.11: 2D projections of volumetric test images.

The volumetric imaging system assessment problem can be defined as a quantification of the system when no reference is available; for such a problem, *ITU-R* recommends the methods described in the *ITU-R* report *BT.1082-1* [69] and pair-wise comparison method is chosen.

The assessment was carried out by 25 subjects: 17 male and eight female, expert and non-expert, with normal or corrected vision (*BT.500-13* states that both experts and non-experts may be observers and at least 15 assessors should participate).

6.4.1 Method

The pair-comparison method is described in *BT.1082-1* report and is carried out by showing the test-subject a pair of pictures or sequences. The test-subject compares pictures by a previously defined standard of judgement (criterion or question, e.g. which picture feels more volumetric?") and chooses one picture of the pair as "the winner." The test-subjects are presented with every pair combination of pictures in random order (similar to a round-robin sports tournament). The results of each pair winners are summarized in a frequency matrix M (also called dominance matrix or count matrix). The final size of M is $t \times t$, where t is the number of different pictures or sequences under testing. For t different pictures, the test-subject must analyze $N = \frac{t \cdot (t-1)}{2}$ picture pairs and determine a preferred picture out of a single pair. The frequency matrix is analyzed using the *Bradley-Terry score* (BTS) model. The *MATLAB* code for *BTS* ranking calculation is based on *Masaoka K., et al* [59].

6.4.2 Stimulus Preparation

Three volumetric images are selected for the test that represent various scenes: a synthesized knot (Fig. 6.11(a)), a lung blood vessel system (Fig. 6.11(b)) and a rendering of a skull (Fig. 6.11(c)).

A single session for one volumetric image consists of the following three parameter tests:

- 1. Distance between layers assess the impact of the distance between depth layers. Test images are prepared by changing the active depth layer distance.
- 2. Spatial aspect ratio assess the impact of the spatial aspect ratio. Test images are prepared by changing the horizontal and vertical size, while maintaining a fixed depth;
- 3. Depth aspect ratio assess the impact of the depth aspect ratio. Test images are prepared by changing the number of depth layers.

All volumetric scenes (three images and three parameters for each image) are prepared in advance and the test-subjects are shown static volumetric image pairs. Each image is preprocessed as described in parameter tests and no additional processing is used (no rotation, scaling or translation among parameter test images).

6.4.3 Results and Analysis

6.4.3.1 Distance between layers

Figure 6.12(a) shows the BTS (ranking) of the variants for each test image. The knot and lungs show a constant score of -1 to -2 for all distance variants. However, the skull image shows a linearly increasing score, which increases as distance decreases. This shows that results are dependent on the



Figure 6.12: Bradley-Terry score (ranking) for three tests representing 3D perception score.

scene and if the test-subjects can associate the scene with a real life object.

6.4.3.2 Spatial aspect ratio

Figure 6.12(b) shows that there is a characteristic local optimum point, which is different among the test images with the exception of the knot image that does not show a local optimum point. The image of the lungs has an optimum at around 65 % x y scale ratio, meaning that test-subjects felt the most comfortable with this x y z aspect ratio. The skull has an optimum of around 50 % most resembling a real life object.

The test-subject feedback during this test expressed that they cannot always answer the question truthfully since the smaller sized volumetric object is not as perceivable as the full sized object.

6.4.3.3 Depth aspect ratio

Figure 6.12(c) shows that for all images the test-subjects strongly preferred the higher number of shutters or the deeper volumetric image. The results for the skull image show a strong logarithmic characteristic at 5 and 8 depth layers followed by linear region from 14 to 20 depth layers, suggesting that the test-subjects felt comfortable observing the volumetric image. The knot and lungs still show linear growth in the same region.

6.5 Summary and Conclusions

User evaluation shows the volumetric perception score is impacted not only by the parameter variance but also by the volumetric scene itself. For example, if the volumetric object is a real life object then it is easier for the test-subjects to evaluate the variants.

The spatial aspect and depth aspect ratio tests can be combined (spatial aspect ratio test continues stretching the object depth-wise, similarly as in the depth aspect ratio test) and suggests that there is an optimum point for the 3D perception score. Based on the test-subject reactions, it seems that this optimum point is where the object is shown with its real, actual spatial aspect ratio. This is abundantly apparent and most strongly shown for skull and lungs test images (Fig. 6.12(b)).

The depth aspect ratio test shows that the number of layers is logarithmic for real life objects and linear for synthesized objects. This partially supports the proposed theory in Chapter 4, that the 3D perception score is a logarithm of number of depth layers. Pairwise comparison analysis result (BTS score) output results as a logarithm from fraction $0 \le p \le 1$ thus, the graphic appears offset but the curve is similar.

In a situation where the volumetric image is not a real or recognizable object but some scanned reconstructed volumetric data set (e.g. ultrasound), the user should first be trained to use a volumetric display (similarly as they are trained to use 2D displays for these technologies).

Conclusions

Multi-planar volumetric technology development previously had been based on trial and error methodology by demonstrating the technology in prototype devices. The devised mathematical expressions and mathematical model allows for in-depth analysis of the technology (operational parameters and configuration), as well as partial optimization of one of the output parameters for a given set of input parameters and defined requirements (minimum or maximum) for other output parameters.

Technology analysis shows a need for the light modulation method that is capable of producing grayscale colors at high refresh rates and for a set of input parameters (for example, $1024 \times 768 \times 20$ volumetric resolution and 8b color depth cannot be produced by the well known pulse-width modulation method with currently available spatial light modulators, while light source intensity modulation method produces 25 % light intensity of pulse-width modulation). Note that a novel mixed light modulation method has been developed as a result of this work. This method produces higher light intensity than the light source intensity modulation method. Although the method is developed for multi-planar volumetric technology, it is not limited to it. The method can be applied for different purposes, applications and technologies wherever grayscale color modulation is required.

Implementation of an experimental device is a technologically challenging task. It requires integration of a spatial light modulator and light sources with a real time volumetric data receiver and mapper. An FPGA integrated circuit allows one to rapidly integrate, prototype and verify required signal mapping algorithms for a volumetric imaging system. The experimental device also includes a real time volumetric data transfer, which is not a common feature for volumetric display technology demonstration devices. It enables one to show the observer a real time volumetric data stream from the source.

The building of the experimental device allowed me to carry out a user-evaluation test. This test gathers user-feedback for the device operational parameters mainly on voxel volumetric density and depth aspect ratio. The results show that there is a logarithmic relation between 3D perception and depth aspect ratio and 17 to 20 depth layers are sufficient for 1024×768 resolution (400mm $\times 300$ mm $\times 100$ mm physical size ratio) for certain applications (e.g. observation of generic 3D objects). The test has shown that the test-subjects preferred that volume size ratio allowed them to observe the 3D object in a natural aspect ratio (meaning, that the object is not scaled within volume in any dimension).

In sum, this thesis introduced mathematical analysis and implementation of a multi-planar experimental device. It was also shown that this device can be used in industry to create and tailor to an industry-specific or requirement-specific volumetric display device.

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