# Passive Power Decoupling Approach for Three-Level Single-Phase Impedance Source Inverter Based on Resonant and PID Controllers

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***Abstract*— Single-phase inverter suffers from double-frequency power ripples in the input side transferred there from the ac-side. To mitigate this ripple, two types of power decoupling approaches can be applied: passive power decoupling and active power decoupling. We present a technique of passive power decoupling realized by modifying the control strategy. The main idea is to produce the time-varying shoot-through duty cycle to charge and discharge impedance capacitors when needed in the desired sequence for mitigating input power ripple without deteriorating the output power quality. The main contribution of the paper is in the determination of the parameters of a regulator taking into account the dynamic feature of the quasi-Z-source network. The validity of the proposed control strategy was confirmed by simulation results in PSCAD. The results show that this strategy can be applied for practical applications.**

***Keywords — passive decoupling; single-phase inverter; PR controller; double-frequency ripple; distorted grid; quasi-Z source.***

## I. INTRODUCTION

During the two last decades, the integration of impedance networks in different fields of application, in particular in Photovoltaic (PV) systems, has been under wide discussion. Different configurations of impedance networks proposed in [1]-[8] allow preventing limitations of the Voltage Source Inverters (VSIs). The Shoot-Through (ST) state is introduced in the system in order to provide boost function without an additional conversion stage. The ST improves the reliability of the system because of absence of any forbidden states.

The qZ-source Neutral-Point-Clamped (NPC) inverter presented in [9] allows use of the single or separated input source(s) to reduce the voltage stress across the switching devices, thus increasing the switching frequency.

Another important feature of the inverter is the capability of injecting current into the distorted LV grid with the required quality set by international standards such as IEEE-519 [10]. Different types of controllers are used to control the quality of the output current injected [11], [12]-[14]. The PR controller looks most promising since it can provide stable fundamental current injection along with Harmonic Compensation (HC) [15].

At the same time, the single-phase system suffers from such drawback as Double-Frequency Ripple (DFR) of input power. Several strategies are reported in the literature to reduce the DFR [16], [17]. These strategies are divided into two types: passive decoupling [18] that means the system has no additional switching devices and active decoupling [19], [20] containing additional switching devices. This paper focuses on passive power decoupling. The purpose of passive power decoupling is to maintain the average voltage of the dc-link with limited second-order fluctuations across it to reduce the same in the input power. Most of the approaches are based on a modified control strategy without configuration changes[18].

Also, the mitigation of input power pulsation can be achieved by means of increasing the values of the passive components [21], [22]. At the same time, it is evident that the size of these components will be larger.

The main problem here is in the oversized passive components used for simulation and experimental verification of the proposed algorithms [16], [18], [21].

The aim is to develop a novel approach based on resonant and PID controllers for passive decoupling. It is clearly demonstrated that such approach is capable of mitigating DFR in the case of optimized passive elements.

## II. CASE STUDY SYSTEM DESCRIPTION

The case study system is depicted in Fig. 1*a*. It consists of the Three-Level (3L) single-phase Neutral-Point-Clamped (NPC) quasi-Z-Source Inverter (qZSI) connected to the distorted grid through an LCL-filter. This topology is described in [23]. Grid voltage contains 5$^{th}$ harmonic that is about 3% from the fundamental one. A PV installation of 10 serial modules is a voltage source for the selected topology. The calculation of passive components is presented below, with summarized values given in Table I.

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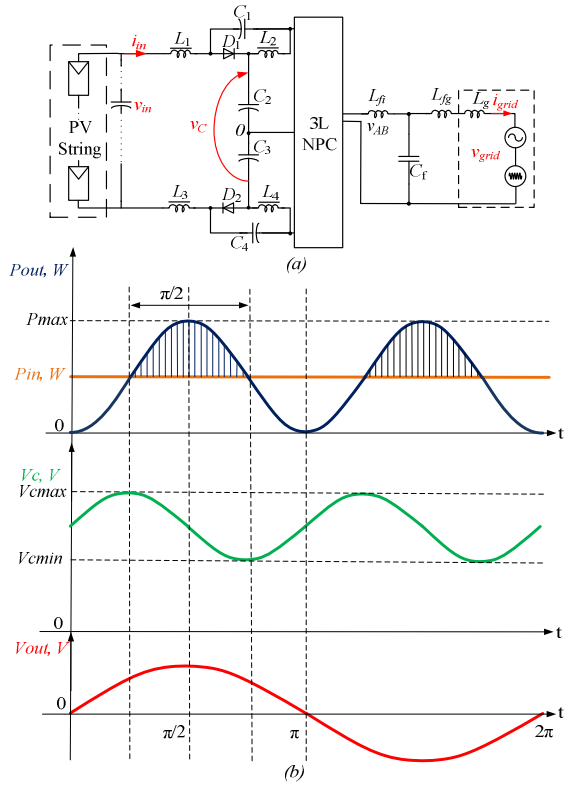


Fig. 1. Single-phase PV system using 3L NPC qZSI *(a)*; idealized waveforms of the output power along with desirable input power, voltage across impedance source capacitors and grid voltage over one line cycle *(b)*.

### A. *Passive elements estimation*

The following assumptions were accepted for the topology studied: $C_1=C_2=C_3=C_4=C$; $L_1=L_2=L_3=L_4$; in the steady state mode, the inductors current is equal; therefore, the capacitors current is equal as well. It will be valid under proper control strategy discussed in the next section. The minimum value of the ST duty cycle ($D_{min}$) depends on the value of the input voltage ($V_{in}$) and the desired minimum value of the output voltage ($V_{dc\_min}$):

$$D_{min} = 0.5 \cdot (1 - \frac{V_{in}}{V_{dc\_min}}). \quad (1)$$

This value should exceed zero to ensure that PR controller operates in linear range.

The average voltage across the capacitors of the qZS network depends on the average value of ST duty cycle ($D$). The average voltage across the capacitors $C_1$, $C_2$, $C_3$, $C_4$ is expressed as [23]:

$$V_{C2} = V_{C3} = \frac{1-D}{1-2D} \cdot \frac{V_{in}}{2}, \quad (2)$$

$$V_{C1} = V_{C4} = \frac{D}{1-2D} \cdot \frac{V_{in}}{2}. \quad (3)$$

Fig. 1*b* shows the idealized waveforms of the output power along with desirable input power, voltage across impedance capacitors and grid voltage over one line cycle ($f_{line}=50$ *Hz*).

The time $\pi/4<t<3\pi/2$ corresponds to the realizing energy mode. During that time, capacitors are discharging to maintain the input power at the average value. The time $3\pi/2<t<5\pi/4$ corresponds to the storage energy mode. During that time, capacitors are charging for the same reason.

According to Fig. 1*b*, the frequency is fixed at the double line frequency and the amplitude is $\pm 100\%$ of the output average power (neglecting losses). It is assumed that the voltage ripple across the capacitors will be distributed evenly.

$$\Delta V_{C1} = \Delta V_{C2} = \Delta V_{C3} = \Delta V_{C4} = \frac{\Delta V_{dc}}{4}, \quad (4)$$

where $\Delta V_{dc}$ is available pulsation in the dc-link.

The maximum and minimum voltages across the capacitors are:

$$V_{C1\_max} = V_{C1} + \frac{\Delta V_{C1}}{2};\ V_{C2\_max} = V_{C2} + \frac{\Delta V_{C2}}{2}, \quad (5)$$

$$V_{C1\_min} = V_{C1} - \frac{\Delta V_{C1}}{2};\ V_{C2\_min} = V_{C2} - \frac{\Delta V_{C2}}{2}. \quad (6)$$

The input power ripple is calculated according to the following equation:

$$\Delta P = \frac{2}{\pi} \int_0^{\pi/2} (P_{max} - P_{in}) \sin(2\omega t) d\omega t. \quad (7)$$

The energy that must be stored in the impedance capacitors in order to mitigate the ripple is defined as:

$$\Delta E = \Delta P \cdot \frac{T}{4} = \frac{P_{in} T}{2\pi}, \quad (8)$$

where $T$ is the fundamental period.

This energy is distributed between capacitors $C_1$ and $C_2$ according to the voltage variation:

$$\Delta E_1 = \frac{C(V_{C1\_max}^2 - V_{C1\_min}^2)}{2} = C \cdot V_{C1} \cdot \Delta V_C, \quad (9)$$

$$\Delta E_2 = \frac{C(V_{C2\_max}^2 - V_{C2\_min}^2)}{2} = C \cdot V_{C2} \cdot \Delta V_C. \quad (10)$$

Finally, the total energy can be expressed as:

$$\Delta E = 2\Delta E_1 + 2\Delta E_2 = 2C \cdot V_{C1} \cdot \Delta V_C + 2C \cdot V_{C2} \cdot \Delta V_C. \quad (11)$$

From (11), the value of the capacitor can be calculated:

$$C = \frac{P_{in} \cdot T}{4\pi \cdot \Delta V_{dc} (V_{C1} + V_{C2})}. \quad (12)$$

Considering that DFR is compensated by the control system and capacitors, the inductor of the impedance network can be selected taking into account high frequency current ripple only. The following expression is presented in many papers:

$$L_1 = L_2 = L_3 = L_4 \geq \frac{V_{in}^2 \cdot (1-D) \cdot D}{2 \cdot P_{in} \cdot f_S \cdot K_I \cdot (1-2 \cdot D)}, \quad (13)$$

where $K_I$ is a current ripple factor and $f_S$ is switching frequency.

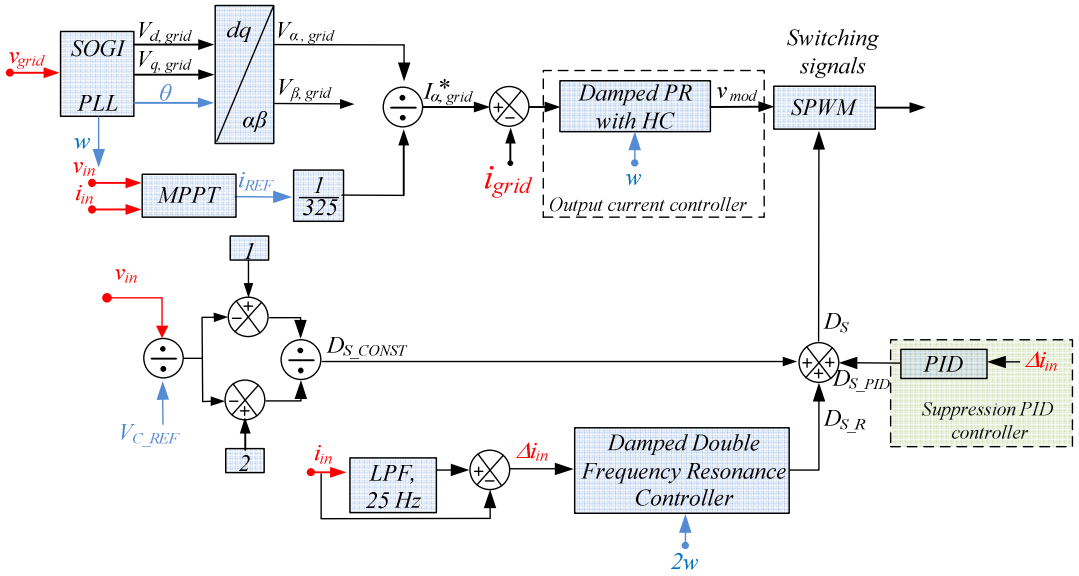


Fig. 2. Block diagram of the proposed control strategy.

## III. CONTROL SYSTEM DESCRIPTION

The proposed control strategy is presented in Fig. 2. The control system can be divided into two parts. The first part provides the desirable value of the dc-link voltage, the other one controls the quality of the output current, which will be injected into the distorted grid.

### A. *Output current controller*

In order to produce the output current that will be injected into the distorted grid with THD that satisfies the international standards (it should be less than 5%), the LCL output filter and damped PR controller with the Harmonic Compensation (HC) approach were applied. HC was applied to attenuate the value of the 3rd, 5th, 7th, 9th order harmonics. Detailed tuning of the PR controller for 3L NPC qZSI is discussed in [12]. The damped PR controller was selected because it provides high gain at the tuning frequency over a wider band in comparison with the conventional PR controller. Comparison of a conventional PR controller and a damped PR controller is presented in [15]. The damped PR controller with the HC transfer function is:

$$G_{dPR\_HC} = K_p + \Sigma \frac{K_H s}{s^2 + 2\omega_{CH} s + \omega_H^2}, \qquad (14)$$

where $H$ is the harmonic order, $w_{CH}$ is cut-off frequency that is defined for each harmonic separately.

The applied control strategy of the SPWM is described in [24]. It is reported that the carrier signal of the ST state has double frequency that relates to the carrier signals of the active state. Thus, in the proposed case, we obtain: $f_{sw}$=*50 kHz* when *Ds=0*, and $f_{sw}$=*100 kHz* when *Ds>0*.

The value of the $D_{S\_CONST}$ provides an average value of the ST required to maintain the average voltage in the inner capacitors $V_C$.

### B. *Resonant suppression controller*

The function of the suppression controller is to acquire the desirable voltage fluctuation in the dc-link that should provide the corresponding voltage fluctuation across impedance capacitors, which allows reducing the power fluctuation in the input side by means of the time-varying of the ST duty cycle. Detailed description is provided in [18] and a resonant controller is proposed in order to suppress the DFR.

The same structure is used in this paper. It has been shown that qZSI may have right half-hand plane zero that limits the system dynamic response. It is a typical non-minimum system. At the same time, the study above has overlooked the possible problems with fluctuations of the input current due to the resonance in the qZS network.

Fig. 3 shows a dynamic model of the input current control loop. It is based on the qZSI small signal model presented in several papers [25]-[27]. It has been shown before that the dynamic behavior of the qZS network strictly depends on the value of the passive components. In the studied case, the value of passive components was selected in order to provide the demanded input and output current quality. At the same time, it cannot be oversized because of practical reasons. As a result, the control system should be tuned for optimal passive component values.

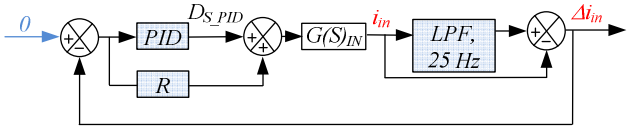


Fig. 3. Dynamic model of the input current control of the qZSI.

The $G(S)_{IN}$ transfer function is derived from the small signal model of qZSI and defines the link between the ST duty cycle and the input current variation. The main purpose of this loop is to suppress possible input current fluctuations connected with the resonance feature of the qZS network.

## IV. Comparative Analysis of the Proposed Control System

This section describes the proposed modification of the control strategy in detail and presents a comparative analysis of our approach and other approaches proposed before.

Fig. 4 shows the root locus diagrams of the dynamic model depicted in Fig. 3. Fig. 4*a* shows the diagram of the system without a PID controller; Fig. 4*b* shows the diagram of the system with a PID controller. As can be seen, the qZ-source inverter with a resonant controller and without a PID controller has roots and zeros that are very close to the axes center. As a result, the system is very sensitive and has complex dynamic behavior.

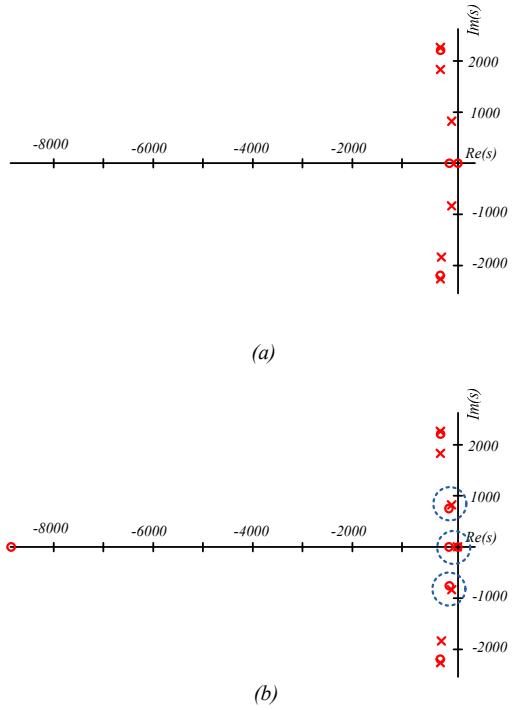


Fig. 4. Root locus diagram of the input current control transfer function without (a) and with (b) PID controller.

Fig. 4*b* shows that adding of a PID controller leads to additional poles and zeros that compensate already existing roots and zeros. As a result, better dynamic performance is expected.

Theoretically, it is possible to tune a PID controller in order to completely eliminate some poles and zeros. But in practical applications it is not possible because of limited passive elements tolerance.

Fig. 5 shows the Bode diagram of the input current control transfer function with a resonant controller but without a PID controller. The system has several resonance peaks, the left one corresponds to the resonant controller, while the right one corresponds to the qZS network resonance frequency.

The main point is that phase shift approaches 180 degrees in the high frequency domain. To shift zeros and poles deeper in the left half-plane, an additional PID controller was applied. The Bode diagram of PID controllers is shown in Fig. 6 and the body diagram of the open loop full transfer function is shown in Fig. 7.

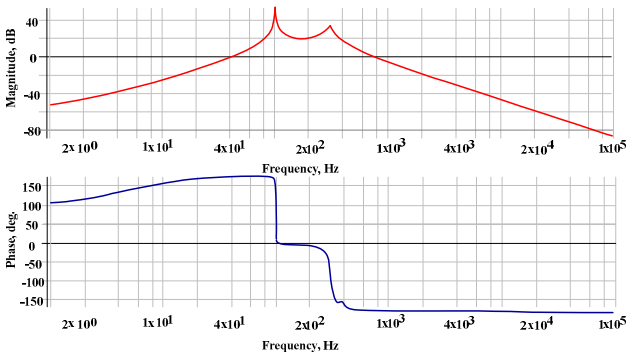


Fig. 5. Bode diagram of the open loop input current control transfer function with a resonant controller.

It can be seen that the PID controller introduces an additional phase lead and the summarized phase shift is closer to 0 degrees, as depicted in Fig. 7. The PID controller corrects phase shifting along with the smoothest gain in the whole range of the frequency domain. As a result, the system is more stable and predicted.

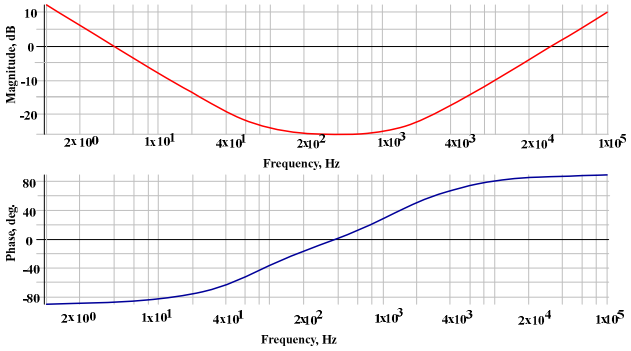


Fig. 6. Bode diagram of the PID controller.

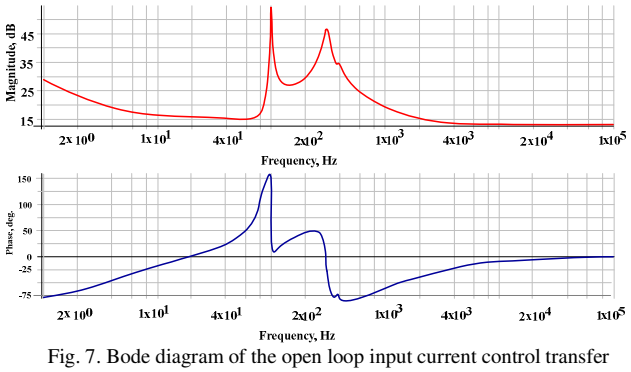


Fig. 7. Bode diagram of the open loop input current control transfer function with resonant and PID controllers.

## V. Simulation Results

Table 1 presents the parameters of the study system that was used in the simulation. Fig. 8 shows the simulation results by using the R term *(a)*; by using the R term with the PID controller *(b)*; transient time by using the R term with the PID controller *(c)*. From top to bottom: input power; summarized voltage across the impedance capacitors and voltage across impedance capacitors separately; ST duty-cycle; grid voltage and current.

TABLE 1. PARAMETERS OF THE 3L SINGLE PHASE QZSI UNDER STUDY

| Parameters | Value |
|---|---|
| *General parameters* | |
| $V_{in}$ | 360 V |
| $V_{Grid}$ | 230 V ac |
| $V_{dc\_ave}$ | 474V |
| $V_{dc\_peak\ to\ peak}$ | 68 V |
| $f_{switching}$ | 50 kHz (100 kHz) |
| $f_{line}$ | 50 Hz |
| *Passive components* | |
| $C_1$, $C_2$,$C_3$,$C_4$ | 0.7 mF |
| $L_1$,$L_2$,$L_3$,$L_4$ | 0.240 mH |
| $R_{qZS}$ | 0.1 Ohm |
| $L_{fi}$ | 0.44mH |
| $L_{fg}$ | 0.22mH |
| $C_f$ | 15, 47 uF |
| $R_f$ | 0.1 Ohm |
| *Input current controller: PID with Resonant controller* | |
| *PID(P)* | 0.05 |
| *PID(I)* | 0.04 |
| *PID(D)* | 5 us |
| *R* | 10 |
| *Output current Proportional-Resonant controller* | |
| $K_P$ | 0.5 |
| $K_1$, $K_3$, $K_5$, $K_7$, $K_9$ | 100; 100, 150, 10, 20 |
| $w_{C1}$, $w_{C3}$, $w_{C5}$, $w_{C7}$, $w_{C9}$ | 0.314, 3.14, 3.14, 3.14, 3.14 |

In Fig. 8*b*, the ripple of the input power is 533 W while the average input power is 1800 W, the ripple across impedance capacitors is 68 V and 17 V across each capacitor separately, which corresponds to the calculation results; the ST duty cycle has high frequency ripple to mitigate fast dynamic pulsation in the input power, the THD of the grid current is about 5%. Fig. 8*a* shows that obviously the R term is not enough to achieve the desired purpose. The ripple of the input power is significant. The quality of the output power was deteriorated. Fig. 8*c* presents the transient time from zero to 0.8 sec. at the moment of time the relay connects the inverter to the grid. At the moment of time 0.2 sec, the inverter starts to operate without the input current mitigation algorithm. Finally, at the moment of time 0.5 sec, the proposed control strategy starts to work.

## VI. CONCLUSIONS

This paper presents the technique of passive power decoupling realized by the modified control strategy based on the resonant with PID controllers. It was shown that the resonant controller cannot provide the satisfied operation mode of the passive decoupling approach due to the possible resonance in the qZS network while the application of the PID controller allows elimination of some zeros and poles, resulting in the stable system.

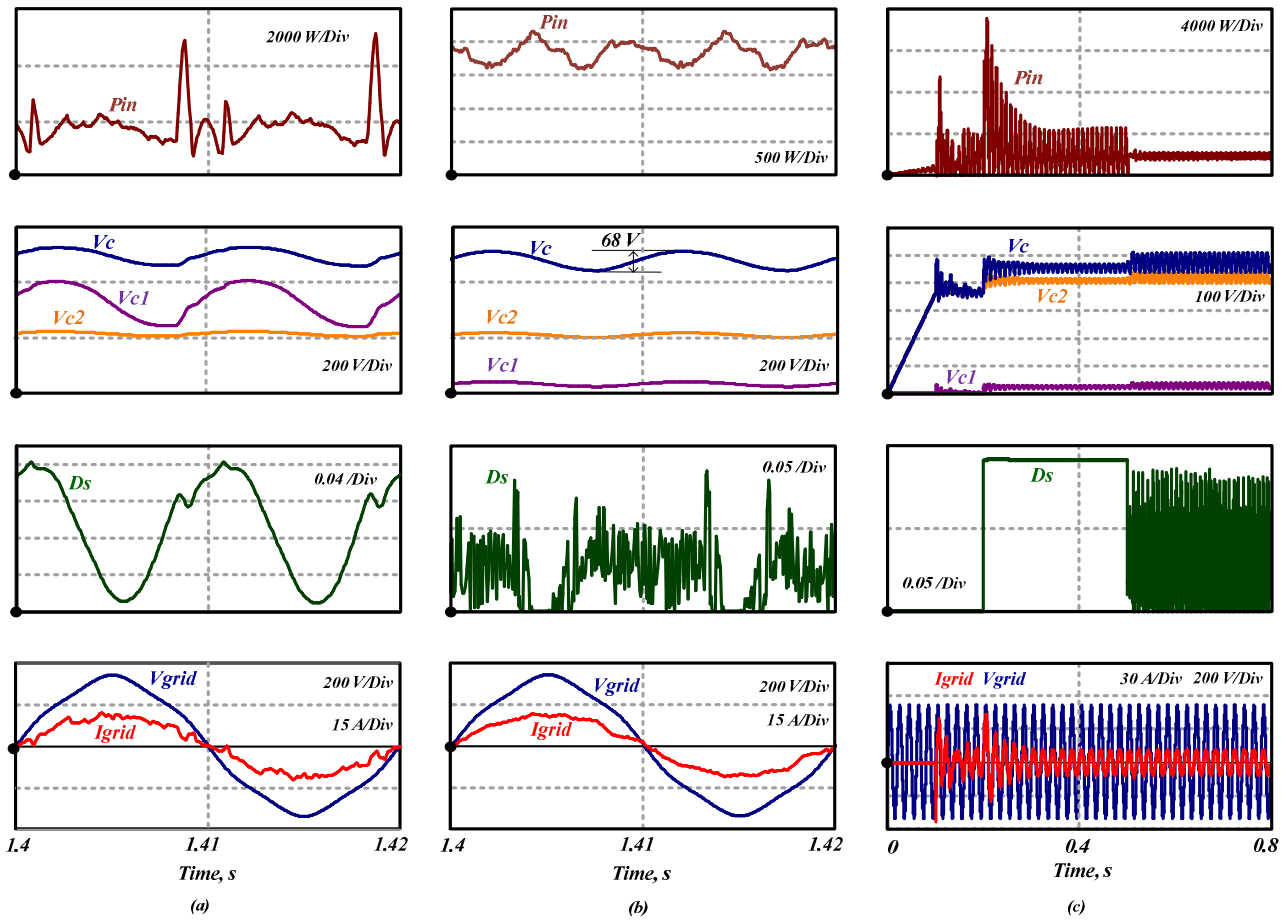


Fig. 8. Simulation results with a resonant controller (a); simulation results with a resonant and a PID controller (b); simulation results of transient time with a resonant and a PID controller (c).

The main idea of passive decoupling is to charge and discharge the impedance capacitors when it is needed. The capacitors of the impedance network should be able to absorb the required ripple energy. Based on this statement, the passive components of the impedance network were calculated. When the grid reduces the consumption of power, the capacitors are discharging and return that energy when the demand of power by the grid is increasing; as a result, the fluctuation of the input power is minimized. For proper work of the resonant term, the ST should exceed zero in all operation modes. Thus, the dc-link voltage is non-fixed, the voltage stress of the switching devices is increasing as compared to the control strategy without the decoupling approach but for low voltage applications and for the 3L converter, this value is not critical. The simulation results confirm the validity of the studied work. The ripple of the input power is 30% at nominal power while the fluctuation confirmed theoretical predictions.

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