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Switch-Off Behaviour of 6.5 kV IGBT Modules in Two-Level Voltage Source Inverter

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Abstract. **This paper presents an analysis of the switch-off process of 6.5 kV/200 A IGBT modules in a two-level half-bridge voltage source inverter. During experiments, it was stated that real switching process is far from ideal switch-off since parasitic inductance and capacitance in the circuit cause voltage spikes and high frequency oscillations during transition processes. Operation states of the inverter are described and analyzed. Experimental and simulation results are compared, the main transients are analyzed and mathematically expressed and possible problems and solutions are discussed.**

Keywords: **pulse width modulated power converters, insulated gate bipolar transistor, freewheeling state, oscillations**

I. INTRODUCTION

Recent advancements in power electronic technologies have made further optimization possibilities in high-voltage high-power converters available. The introduction of 6.5 kV IGBTs has enabled simple and reliable two-level half-bridge voltage-source inverter (VSI) topologies to be implemented for the rolling stock auxiliary power units. Investigations have shown that an experimental converter based on very simple half-bridge topology with two Infineon 200 A/6.5 kV IGBTs (FZ200R65KF1) is capable of providing required performance within the whole range of rolling stock supply voltage of 2.2…4.0 kV and a wide power range – 10…70 kW [1]. Such inverters (Fig. 1, Table I) are very simple in control and protection, have reduced component count and provide good reliability. Converters with described topology and switching elements are perfectly suitable for use in isolated DC/DC rolling stock converters as front-end converters of auxiliary power supplies.

Main problems of this topology are high power losses in semiconductors due to hard switching and consequently, limited switching frequency because of thermal issues. This imposes increased requirements on passive components of the converter. These downsides are related to the common peculiarity of half-bridge topologies – voltage spikes after transistor turn-off (Fig. 2). The voltage spikes are followed by oscillations, obviously caused by presence parasitic capacitive and inductive circuit elements. This paper describes the reasons of these processes in high voltage (≥2 kV) high power (≥20 kW) half-bridge inverters with modified sine wave output operation as well as their effect on the overall performance of the converter.

II. OPERATION OF THE TWO-LEVEL HALF-BRIDGE INVERTER

Two equal capacitors C_1 and C_2 are connected in series across the DC input voltage source, providing a constant potential of the one-half U_{IN} at their junction. Two-level half-bridge inverter has two operating states: active states (*A1*, *A2*) and a freewheeling state (*FRW*). During active states, the two transistors *TT* (top switch) and *TB* (bottom switch) are switched alternately, providing positive and negative square-wave impulses with the amplitude of $U_{IN}/2$ on the isolation transformer *TX* primary winding (Table II). Even a short-time simultaneous opening of the two transistors will result in

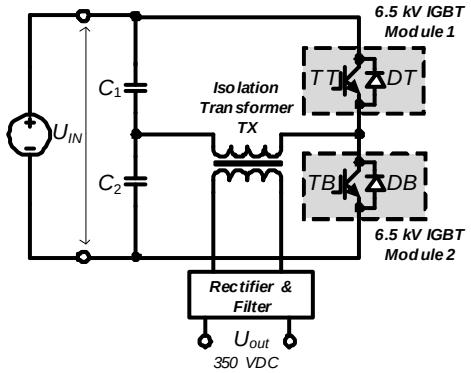

Fig. 1. Two-level half-bridge 6.5 kV IGBT based converter.

TABLE I
MAIN PARAMETERS OF THE HALF-BRIDGE CONVERTER

Parameter	Symbol	Value
Maximum input voltage, V	$U_{IN\,(max)}$	4000
Minimum input voltage, V	$U_{IN\,(min)}$	2200
Nominal input voltage, V	$U_{IN\,(nom)}$	3000
Output power, W	P_{out}	50000
Nominal output voltage, V	U_{out}	350
Switching frequency, Hz	f_{SW}	1000

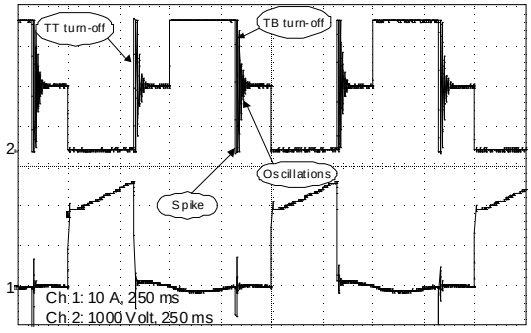

Fig. 2. *TT* IGBT collector-emitter voltage (top) and current (bottom) waveforms during the test of the prototype (U_{IN}=3000 V; f_{SW}=1 kHz, D=0.32, 46 % load).

TABLE II

SWITCHING STATES OF A TWO-LEVEL INVERTER

Inverter state	Transistor state		Output Voltage
	TT	*TB*	
A1	ON	OFF	$-U_{IN}/2$
FRW	OFF	OFF	0
A2	OFF	ON	$+U_{IN}/2$

TABLE III

PARASITIC AND LOW-SIGNAL CAPACITANCES OF THE IGBT

Capacitances	Designation
C_{GE}	Gate-emitter capacitance
C_{CE}	Collector-emitter capacitance
C_{GC}	Gate-collector capacitance (Miller capacitance)
$C_{IES} = C_{GE} + C_{GC}$	Input capacitance
$C_{RES} = C_{GC}$	Reverse transfer capacitance
$C_{OES} = C_{GC} + C_{CE}$	Output capacitance

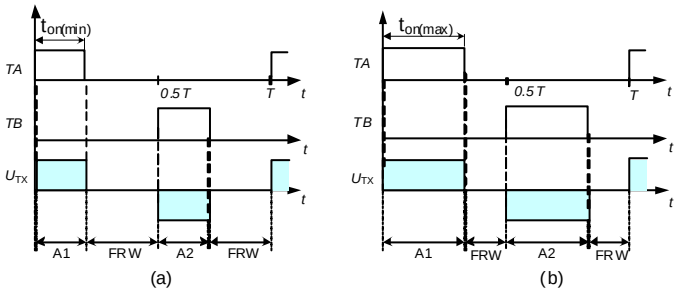

Fig. 3. Switching waveform of a two-level half-bridge DC/DC converter: maximal input voltage (a) and minimal input voltage (b).

short-circuit, therefore the maximum on-state time t_{on} of the transistor control pulse should not exceed 80% of the half period (Fig. 3). This implements a freewheeling state when both transistors are off. During this state, the output voltage is zero [2].

III GENERALIZED EQUIVALENT CIRCUITS OF A TWO-LEVEL HALF-BRIDGE CONVERTER

In a real inverter, every detail has stray inductance, resistance and capacitance. These parasitic components have an influence on the performance and if not considered, could lead to dangerous overvoltages, EMI problems and damage of the inverter. Switch-off process is most influenced by the stray inductance of the isolation transformer and parasitic inductance of the wiring as well as the junction capacitances of HV IGBT modules.

A. Structure of the IGBT module

The switching behaviour (turn-on and turn-off) of an IGBT module is generally determined by its structural, internal capacitances (charges) and the internal and outer (gate drive) resistances (Fig. 4, Table III).

The gate resistor R_G is limiting the magnitude of the gate current I_G, which dictates what the time is needed to charge/discharge IGBT input capacitance C_{IES} during turn-on and turn-off. Generally, a turn-off resistor must have a higher value than a turn-on one.

TABLE IV

DATASHEET VALUES OF INFINEON FZ200R65KF1 MODULES

Parameter	Symbol	Value
DC collector current, A	I_C	200
Collector-emitter blocking voltage, V	I_{CES}	6500
Maximum junction temperature, ºC	Tj_{max}	125
Input capacitance, nF	C_{IES}	28
Turn-on delay time, μs	$t_{d(on)}$	0.75
Rise time, μs	t_r	0.40
Turn-off delay time, μs	$t_{d(off)}$	6
Turn-off fall time, μs	t_f	0.5
Diode peak reverse-recovery current, A	I_{rm}	270
Typical turn-on gate resistance, Ω	$R_{G,on}$	13
Typical turn-off gate resistance, Ω	$R_{G,off}$	75

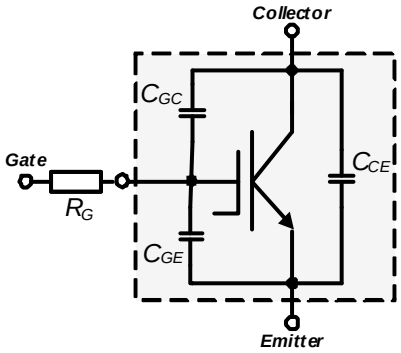

Fig. 4. Equivalent intrinsic capacitances of the IGBT.

In high frequency inverters, overvoltage caused by the energy stored in the stray inductance of a transformer could cause a high voltage spike on the IGBT. However, this process does not occur in the investigated inverter since the nominal switching frequency f_{SW} is only 1 kHz and freewheeling diode starts to conduct before noticeable overvoltage spike occurs. It is evident that the increased gate resistance slows the IGBT switching process, limiting overvoltage, on the other hand, increasing switching losses. Reference values of Infineon FZ200R65KF1 modules are presented in Table IV [3][4]. IGBT parasitic capacitance values are dependent on the transistor module type and not presented in the datasheet of FZ200R65KF1, complicating further calculations.

B. Equivalent parameters of the converter

Based on the parameters, most influential to the active and freewheeling states, the simplified equivalent circuits for the considered half-bridge converter were elaborated.

The value of the equivalent load resistance can be obtained from [5]:

$$R_L = \frac{U^2_{Prms}}{P_{Tr}}, \quad (1)$$

where U_{Prms} is the transformer primary rms voltage and P_{Tr} is the power of the isolation transformer (neglecting losses).

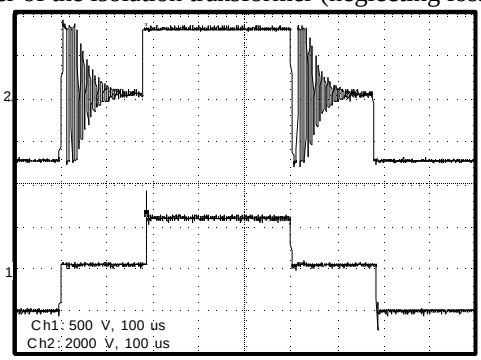

Fig. 5. Isolation transformer primary (top) and secondary voltage (bottom) waveforms during the test of the prototype (U_{IN}=3000 V; f_{SW}=1 kHz, D=0.32, 46 % load).

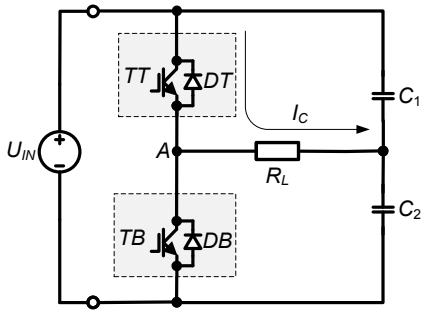

Fig. 6. Active state of the *TT* transistor in the two-level half-bridge converter.

The transformer primary rms voltage is proportional to the converter input voltage:

$$U_{Prms} = \frac{U_{IN}}{2} \cdot \sqrt{2 \cdot D}\,, \tag{2}$$

As Fig. 5 reveals, the parasitic oscillations occur only on transformer primary winding, hence only primary winding parameters are considered. Freewheeling state model includes a third-order oscillatory circuit. The total parasitic inductance of the equivalent circuit is described by:

$$L_E = \sum_{i=1}^{n} L_i\,, \tag{3}$$

where $L_1 \ldots L_n$ is the inductance of the inverter circuit elements including bus, wiring and contact parasitic inductance, as well as the equivalent stray inductance of the transformer primary. The magnitude of the circuit impedance is:

$$Z_{Tr\_p} = \sqrt{R_E{}^2 + \left(2 \cdot \pi \cdot f_{osc} \cdot L_E - 1/(2 \cdot \pi \cdot f_{osc} \cdot C_{Tr\_p})\right)^2} \tag{4}$$

where f_{osc} is the frequency of parasitic oscillations, R_E is the equivalent active resistance of inverter busbar, wiring and transformer primary winding. Parasitic capacitive component $C_{Tr\text{-}p}$ is generally represented by effective distributed capacitances of the primary winding.

IV Analysis of Freewheeling State of the Two-Level Half-Bridge Converter

Two-level half-bridge inverters have two basic operating states: active state and freewheeling state. During the active state either *TT* or *TB* is turned on. During the active state the current I_C flows through the top or bottom transistor, input capacitors C_1 and C_2 and the primary and secondary windings of the isolation transformer. The active state of the *TT* transistor is presented in Fig. 6. The freewheeling state takes place when both switches are off.

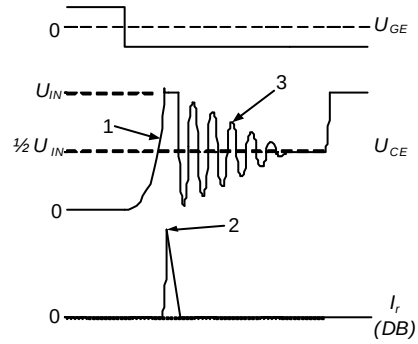

Fig. 7. Generalized representation of the turn-off process of *TT* IGBT. U_{GE} is the gate-emitter voltage of transistor (control signal), U_{CE} is the collector-emitter voltage, I_r is the current impulse through *DB*, events 1-3 are marked.

At the end of the active state, a negative gate control voltage is applied to the *TT* transistor, closing it and starting the freewheeling state (Fig. 7) [6]. The following events can be distinguished:

1. Transistor internal capacitances begin to discharge and the collector-emitter voltage $U_{CE}(t)$ of the IGBT begins to rise. As the current I_C through the transistor decreases, the energy stored in the stray inductance of the power circuit develops a negative voltage potential at point A calculated by:

$$U_{Stray} = L_E \cdot \frac{dI_C}{dt}\,, \tag{5}$$

where L_E is the stray inductance of the power circuit, dI_C/dt is the rate-of-fall of the transformer primary current, Fig. 8(1). This voltage potential is added to the collector-emitter voltage after transistor turn-off:

$$U_{CEpeak} = U_{IN} + U_{Stray}\,. \tag{6}$$

2. After the voltage potential at point A becomes lower than the ground potential of U_{IN}, the current I_r begins to flow through the freewheeling diode *DB* (Fig. 8). The maximal reverse current $I_{r(peak)}$ through the diode at the instant of turn-off is equal to the *TT* collector current $I_{C(max)}$ before turn-off. The current then decays exponentially when $I_r(t) \geq 0$ according to [7]:

$$I_{C(max)} = I_{r(peak)} = \frac{P_{Tr}}{U_{IN} \cdot D} = \frac{U_{IN}}{2 \cdot R_L} \tag{7}$$

$$I_r(t) = I_{r(peak)} \cdot e^{\frac{-R_E \cdot t}{L_E}} - \frac{U_{IN}}{2 \cdot R_E} \cdot \left(1 - e^{\frac{-R_E \cdot t}{L_E}}\right) = \left(I_{r(peak)} + \frac{U_{IN}}{2 \cdot R_E}\right) \cdot e^{\frac{-R_E \cdot t}{L_E}} - \frac{U_{IN}}{2 \cdot R_E}. \quad (8)$$

The current follows this equation until it equals zero.

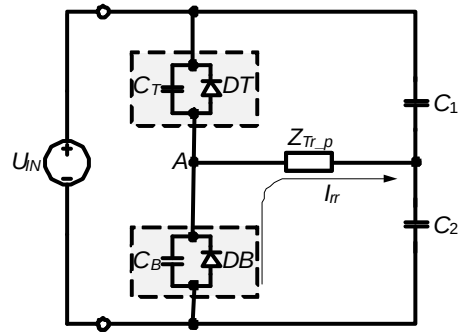

Fig. 8. Reverse current of the *DB* diode after *TT* transistor switch-off.

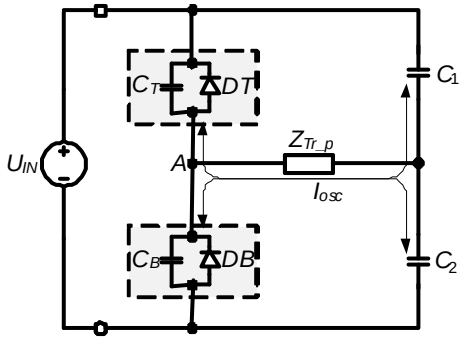

Fig. 9. RLC circuit causing the oscillations after IGBT switch-off.

The current then remains at zero until the next diode conduction. The duration t_{Ir} of decaying reverse current is described by equation:

$$t_{I_r} = \frac{L_E}{R_E}\left[\ln\left(I_{r(peak)} + \frac{U_{IN}}{2 \cdot R_E}\right) - \ln\left(\frac{U_{IN}}{2 \cdot R_E}\right)\right]. \quad (9)$$

3. After depletion of the energy stored in stray inductance, the reverse current through *DB* stops. The output capacitances of IGBT modules C_T and C_B together with the stray inductance L_E and equivalent impedance of circuit $Z_{Tr\text{-}p}$ form an oscillating RLC circuit (Fig. 9). C_B and C_T begin to charge and discharge. Voltage and current in this RLC circuit oscillates until being damped by R_E and the voltage potential of point A becomes equal to *1/2* U_{IN}.

V ELABORATION OF THE SIMULATION MODEL

Determination of the parasitic elements causing oscillations requires a simulation model to be elaborated. The oscillation frequency of the damped circuit f_{osc} is [8]

$$f_{osc} = \frac{1}{T_{osc}} = \frac{\omega}{2 \cdot \pi} = \frac{\sqrt{\omega_0^2 - \delta^2}}{2 \cdot \pi}, \quad (10)$$

where undamped resonance frequency $\omega_0 = 1/\sqrt{L_E \cdot C_E}$, attenuation $\delta = R_{HF}/(2 \cdot L_E)$, R_{HF} is equivalent high-frequency resistance and C_E is generally represented by the sum of equal paralleled IGBT parasitic capacitances C_T and C_B.

TABLE V
VALUES OF SIMULATION PARAMETERS

Parameter	Symbol	Value
Input voltage, V	U_{IN}	2200…4000
Inverter input capacitances, μF	C_1, C_2	300
IGBT parasitic capacitances, pF	C_T, C_B	450
Equivalent impedance at 310 kHz, Ω	Z_{Tr_p}	81.8
Switch duty cycle	D	0.22…0.4
Switching frequency, kHz	f_{SW}	1…2

According to the measurements, the oscillation frequency is 310 kHz (Fig.7). Oscillation is described by the oscillatory circuit quality factor *Q*:

$$Q = \frac{2 \cdot \pi \cdot f_{osc} \cdot E_s}{P_{osc}} = \frac{1}{R_{HF}} \cdot \sqrt{\frac{L_E}{C_E}} = \frac{\pi}{\ln(U_n / U_{(n+1)})}, \quad (11)$$

where U_n and U_{n+1} are amplitude values of voltage oscillations separated by the time interval of T_{osc}. The equivalent stray inductance L_E can be obtained by

$$L_E = \frac{R_{HF}}{2 \cdot \ln(U_n / U_{n+1}) \cdot f_{osc}}. \quad (12)$$

Equivalent module capacitances can be obtained from the oscillation frequency equation

$$C_T = C_B = \frac{1}{2} \cdot \left(\frac{1}{L_E \cdot (\omega^2 + \delta^2)}\right). \quad (13)$$

The voltage oscillations across transistor after reverse current impulse follow the equation [9]:

$$U_{osc} = \frac{U_{IN} \cdot \omega_0}{2 \cdot \omega} \cdot \cos\left(\omega \cdot t - \arctan\frac{\delta}{\omega}\right) \cdot e^{-\delta \cdot t}. \quad (14)$$

and oscillating current is described by:

$$I_{osc} = \frac{U_{IN}}{2 \cdot \omega \cdot L_E} \cdot \sin \omega \cdot t \cdot e^{-\delta \cdot t}. \quad (15)$$

VI SIMULATION RESULTS

According to the generalized equivalent circuit, a simulation model is created using PSIM software. The simulation model elaborated has the same configuration as the

test prototype in Fig. 1 and includes the values presented in Table V.

Obtained simulation results were compared with laboratory measurements of the converter prototype (Fig. 11). Further, inverter performance was simulated under different operation conditions (Figs. 11-12). The presence of the oscillations showed no significant impact on the performance in the simulations as well as during the laboratory tests. The current amplitude during oscillations remained relatively low; hence, the energy of the oscillations is relatively low as well.

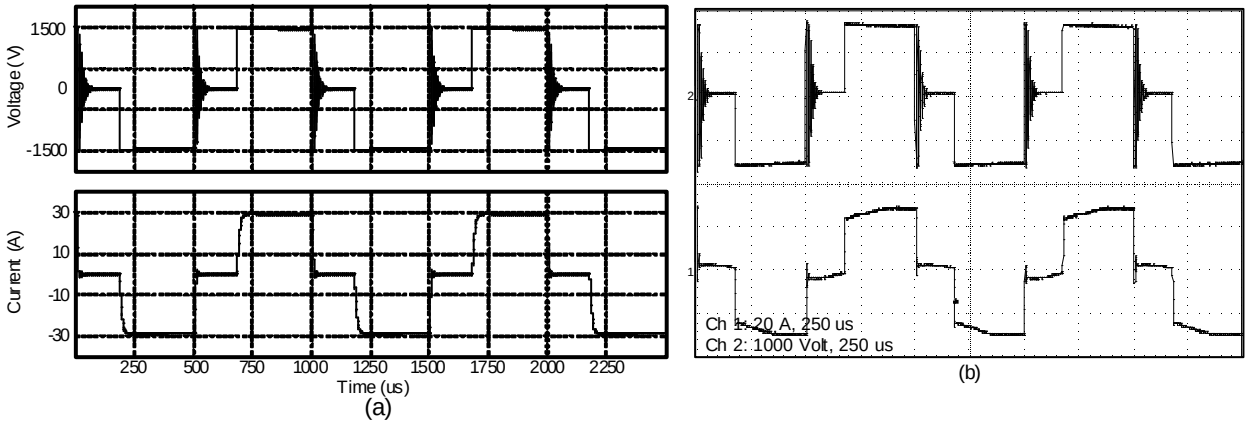

Fig. 10. Simulated (a) and experimental (b) transformer primary voltage (top) and current (bottom) (U_{in}=3000V; f= 1 kHz; D=0.32; R_L=48.4 Ohm).

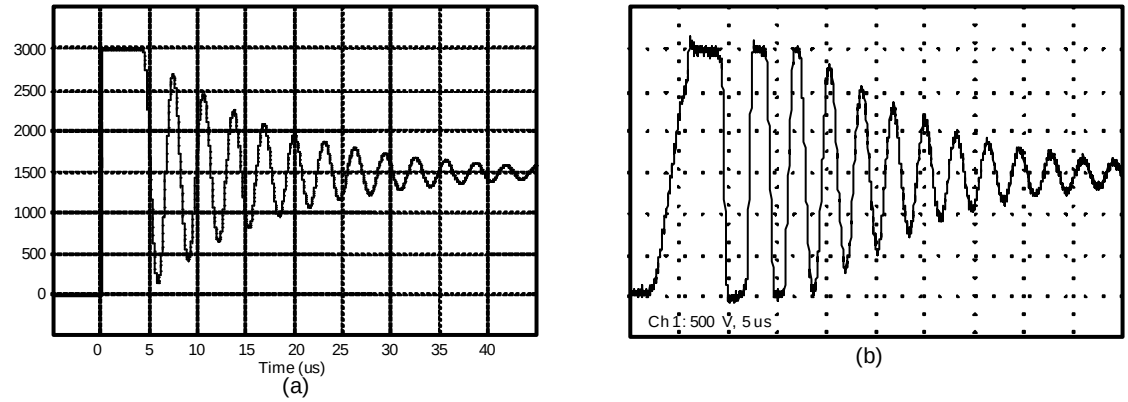

Fig.11. Simulated (a) and experimental (b) *TT* IGBT collector-emitter voltage (U_{IN}=3000 V; f_{SW}=1 kHz, D=0.32; R_E=48.4 Ohm).

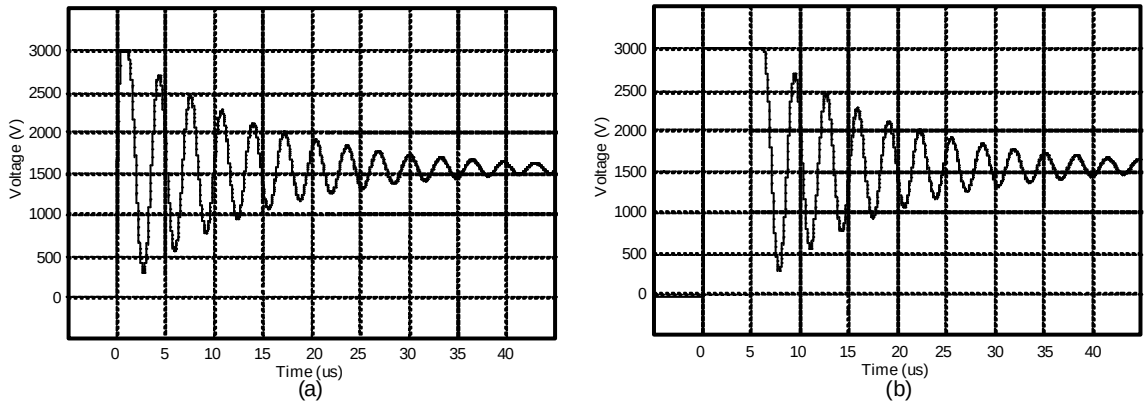

Fig.12. Simulated *TT* IGBT collector-emitter voltage: U_{in}=3000V; f= 1 kHz; D=0.32; R_L=288 Ohm(10% load) (a); R_L=28.8 Ohm (100% load) (b).

VII. CONCLUSIONS

During the laboratory test of the prototype, as well as in the computer simulations, the frequency of oscillations was found independent of the input voltage or the switching frequency of transistors and remained at approximately 310 kHz. The amplitude value of oscillations is proportional to the input voltage. The value of the reverse current impulse depends on the converter output power, i.e. the more energy is stored in the parasitic inductance, the more reverse current is required to deplete it. On the contrary, under light load operation, the duration of reverse impulse is decreased. The simplified simulation model showed similar results compared to the values obtained during the laboratory test of the converter prototype. Although not entirely precise, the simulation model gives an adequate estimation of the processes that occurred during the laboratory tests.

High stray inductance of the isolation transformer results in higher losses as well as voltage and current oscillations after switch-off. Although the frequency of those oscillations is not high enough to generate strong radiated EMI, it can cause some problems with conducted EMI in the contact line. Due to the required high isolation voltage of the isolation transformer, the high stray inductance is hard to avoid, moreover the capacitance of HV IGBT modules cannot be avoided. In the case of the considered high-voltage inverter, these parasitic effects are not dangerous to HV IGBT modules, neither are they dangerous to other circuit elements since they do not create noticeable overvoltage. On the other hand, the losses are increased, thus the nominal switching frequency is limited at 1 kHz. Generally, the ways to reduce the impact of parasitic effects are dissipative snubber circuits and low inductivity busbar system. Due to high-voltage supply, implementation of snubber circuits is complicated and is unlikely to significantly improve the performance of the converter.

ACKNOWLEDGEMENT

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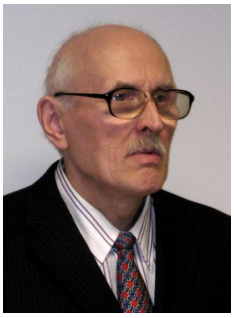

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