RIGA TECHNICAL UNIVERSITY

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Research and Development of Interface Converter for PMSG Based Wind Generator

Doctoral thesis

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ANNOTATION

This doctoral thesis is dedicated to investigation of impedance source DC/DC converter with HF isolation implementation in interface converter for permanent magnet synchronous generator based variable speed wind turbine. The three new topologies of interface converter are proposed for PMSG based VSWT applications. The operation modes of the converters are investigated by means of computer simulations and results have been experimentally verified. The analytical evaluation of losses in active components of power circuit is made to compare feasibility of three circuits for small and micro wind turbine applications. The Laboratory prototype of qZS based DC/DC converter with HF isolation and controlled rectifier has been built and tested.

The first chapter of the thesis is devoted to general overview of wind energy conversion technologies. Wind theory is given and wind velocity distribution is analysed to state the requirements for interfacing converter. Already known wind turbine systems are analysed to select the most suitable one for improvement and investigation. The converter topology with HF isolation transformer was selected for small and micro VSWT applications due to grate flexibility and offered galvanic isolation. The need for improved converter for VSWT applications is stated and main requirements is defined based on PMSG based VSWT characteristics.

The second chapter is devoted to qZS based interface converter investigation and development. The new topologies based on qZS DC/DC converters with HF isolation are offered. These topologies are investigated by means of computer simulation in PSIM software and are verified experimentally.

The third chapter is devoted to new topology of qZS based DC/DC converter with improved voltage boost properties. The potential applications are stated and analysed.

Thesis is written in English, contains: 108 pages, introduction, three chapters, conclusions, 88 figures, 74 formulas, 12 tables, 100 references and 2 appendixes.

ANOTĀCIJA

Šis doktora darbs ir veltīts elektroenerģijas sadales tīkla un mainīga ātruma vēja ģeneratora ar pastāvīgo magnēta sinhrono mašīnu salāgojošā pārveidotāja ar pretestības avota DC/DC pārveidotāju un augstfrekvences izolāciju izpētei un izstrādei. Darbā tiek piedāvāti trīs jauni spēka shēmu varianti mainīga ātruma vēja ģeneratoriem. Darbā ar datormodelēšanas palīdzību tiek pētīti pārveidotāju darba režīmi un modelēšanas rezultāti tiek salīdzināti ar eksperimentālajiem. Jaudas zudumu analītisks novērtējums pusvadītāju elementos tiek parādīts, lai novērtētu piedāvāto shēmu piemērotību mikro un mazas jaudas vēja iekārtām. Pretestības avota līdzstrāvas pārveidotāja laboratorijas prototips tika izstrādāts un pārbaudīts.

Pirmajā nodaļā tiek apskatītas vēja enerģijas izmantošanas paņēmieni. Vēja teorija pamati un vēja sadalījums tiek analizēts, lai noteiktu prasības salāgojošajam pārveidotājam. Jau zināmās pārveidotāju spēka shēmas tiek apskatītas, lai izvēlētos vispiemērotāko pilnveidošanai. Pārveidotāja spēka shēma ar augstfrekvences izolāciju tika izvēlēta tās elastīgo konfigurēšanas iespēju un galvaniskās izolācijas dēļ. Apskatot esošos pārveidotājus tika paradīta nepieciešamība meklēt jaunus shemotehniskos risinājumus un nobeigumā tika definēti pārveidotāja tehniskie parametri, atbilstoši laboratorijā pieejamajam ģeneratoram.

Otrajā nodaļa ir veltīta salāgojošajiem pārveidotājiem ar pretestības avota DC/DC pārveidotāju. Tiek piedāvāti jauni spēka shēmu varianti. Tiek dots piedāvāto spēka shēmu matemātiskais apraksts un veikta to modelēšana PSIM vidē, bet rezultāti tiek eksperimentāli apstiprināti.

Trešajā nodaļā tiek piedāvāts jauna spēka shēma pretestības avota DC/DC pārveidotājam ar komutējamām droselēm. Potenciālās pielietojumu jomas tiek apskatītas un analizētas.

Darbs ir rakstīts angļu valodā uz 108 lapaspusēm, sastāv no ievada, trīs nodaļām un secinājumiem, kā arī tajā ir 88 attēli, 74 formulas, 12 tabulas, 100 literatūras avoti un 2 pielikumi.

ACKNOWLEDGEMENT

Firstly, I would like to thank my supervisor, Prof. Ilya Galkin for support and encouragement during all my studies.

Additionally I would like to thank my colleagues and friends from Institute of Industrial Electronics and Electrical Engineering for support and advice when it was necessary.

Special thanks go to Dmitri Vinnikov and all colleagues from Department of Electrical Drives and Power Electronics of Tallinn University of Technology for theoretical and practical help.

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CONTENTS

INTRODUCTION

Continuous growth of the earth population and improving standards of living are the main driving forces for the continuous growth of the energy demand. Although the energy use per unit of gross domestic product (GDP) is declining in most countries, the GDP increase is faster than efficiency growth, causing to use more and more recourses for energy production. It is forecasted that this trend will continue in the upcoming decades (Fig. 0.1) [11]. Limited availability of fossil energy resources, such us coal, natural gas, oil and nuclear, urge to make use of renewable sources for electric energy generation. Moreover, the use of fossil fuels are connected with greenhouse gas emissions and in case of the nuclear energy, there is a high potential of radiation product leakage that can cause irreversible damage to environment, but used fuel and old utility disposal is connect with high expenses after the closure of nuclear power stations. Environmental aspects and expenses are additional driving forces for technology development of alternative energy usage.

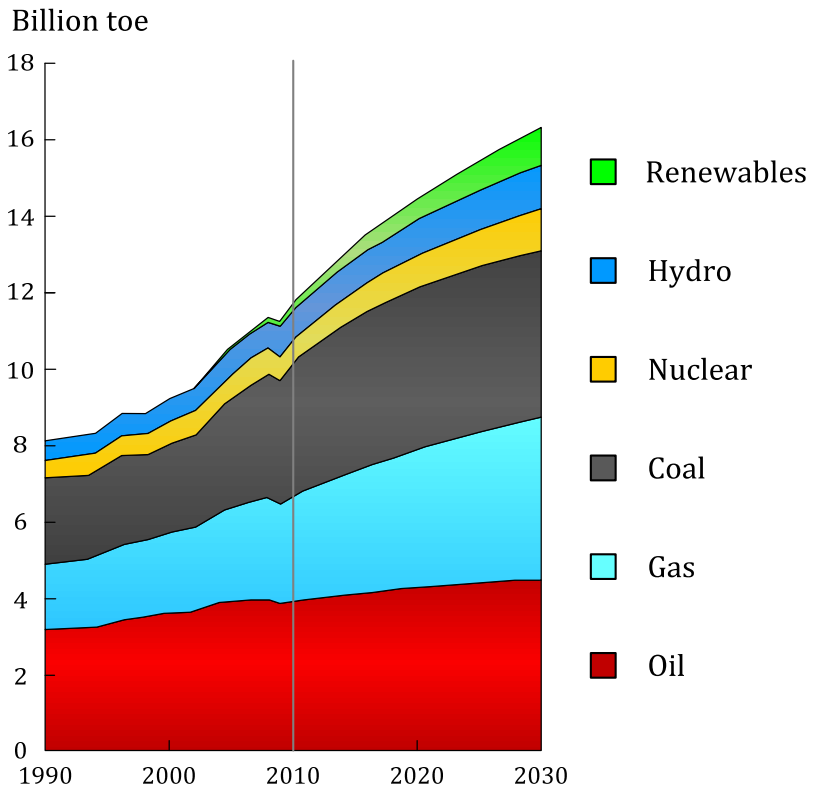


Fig. 0.1. Energy consumption by sources types

The cost of electrical energy from alternative energy sources is major concern that prohibits wider its utilization. This is particularly true for micro and small wind turbine applications due to the low typical installation height and as a result lower average wind speeds that leads to lower produced energy. Since there is no possibility to affect average

wind speeds, the only way how to increase the energy output of wind turbine systems (WTS) is to improve the efficiency of all its components. This dissertation is devoted to new power electronics converter development for micro and small wind turbines.

Wind energy is quite an attractive form of renewable energy especially at high latitudes where feasibility to apply direct solar energy conversion technologies is limited. The commercial potential of wind energy [72 TW] is five times higher than world energy demand in all forms [15]. However, the installed capacity in 2009 was only 159GW and there are the huge potential of grow [54].

The humankind utilizes windmills more than 2000 years. Mainly they were used in water pumping and grain milling applications. The Dutch windmills of different kinds get popularity in the 17th and 18th century in Europe, but the concept of Western mills in the 19th century in the USA. The construction of wind mills that can be seen our days were developed in the 1920s, but commercial interest for wind mills as renewable energy source arise only in the end of last century [35]. Wind mills mainly are utilized for electricity generation nowadays. The installed power starts from few hundred Watts and reach 6 MW for commercially available turbines. 10 MW turbines are in pilot stage for offshore applications. There can be find different classifications of turbines by power and their size in literature and standards [42], but to eliminate misunderstandings the classification given in (Table 0.1) will be used in this thesis.

Table 0.1

The general classification of wind turbines

Scale	Power rating	Rotor diameter
Micro	50 W – 3.5 kW	< 4 m
Small	3.5 kW – 50 kW	4 m – 16 m
Medium	50 kW – 1 MW	16 m – 46 m
Large	> 1 MW	> 46 m

Mechanical energy of wind turbines are converted in electrical energy with help of appropriate generators. Permanent magnet synchronous generators (PMSG) predominate in small turbines and become popular in large power range (Fig. 0.2) due to multipole design that eliminates the need for gearbox [43]. Fig. 0.2. demonstrates the results of commercially available [30] WTS analysis by generator types depending on turbine size. Use of PMSG in WTS is modern trend and thanks to high efficiency [32] they will keep this status in future.

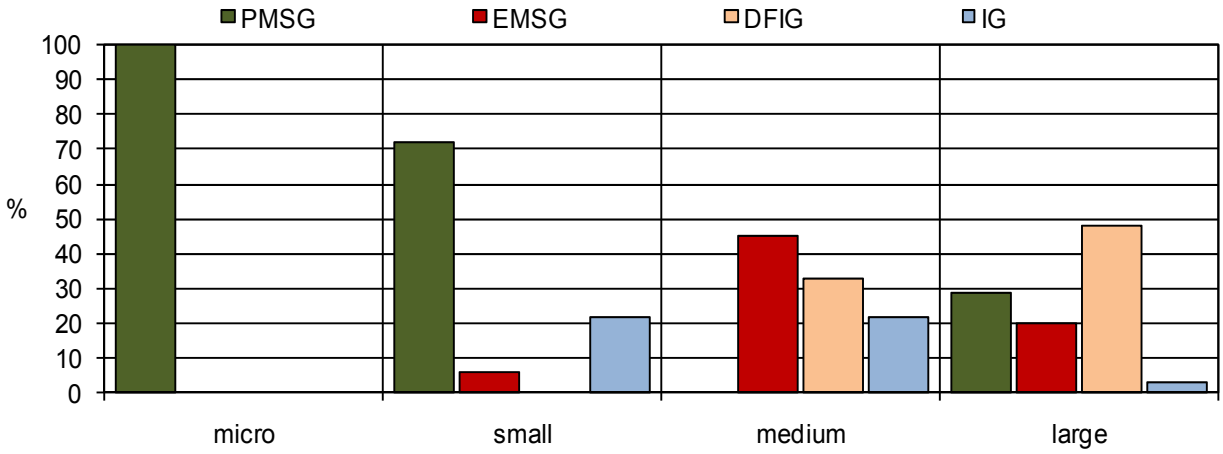


Fig. 0.2. Distribution of generators by type depending on turbine size

Although the energy yield is higher for large inland and off-shore installations, the issue of transmission and distribution losses still is of major concern. Distributed generation and smart grid technologies (Fig. 0.3) are introduced to reduce transmission losses by bringing closer energy generation and utilization and reducing load variations over time. The charging control of the electric vehicles can be the main load balancing feature, and can serve as energy buffer for unpredictable wind energy generation. The rapid popularity increase of electric and plug in hybrid cars will eliminate additional expenses for electric energy storage devices from wind in near future, but utility grid can absorb energy excess during strong wind periods.

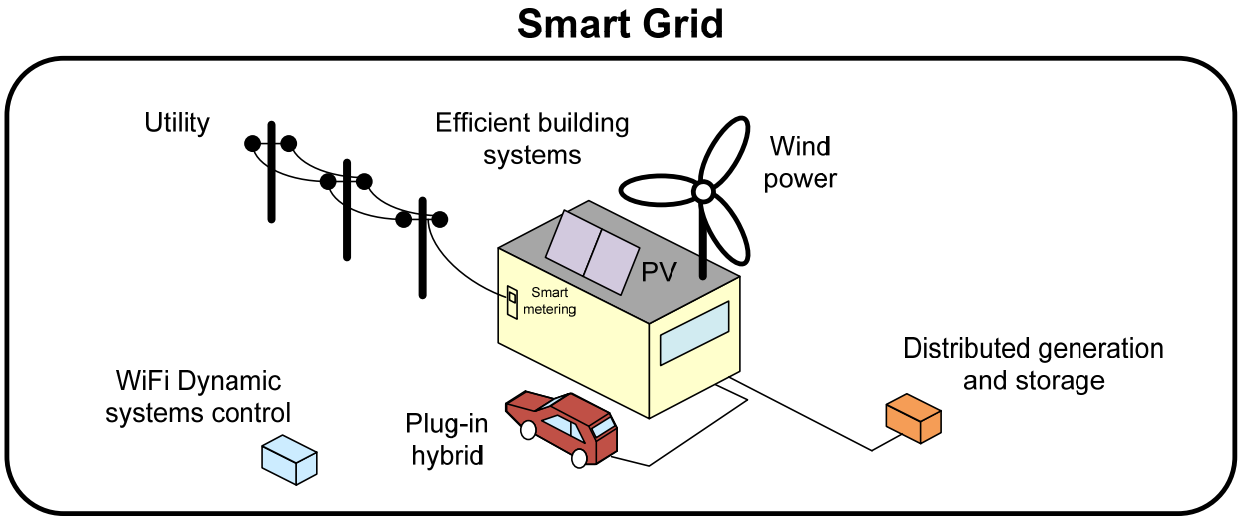


Fig. 0.3. Overview of smart grid structure

DC link utilisation for connection of generating and consuming units is beneficial in smart grids applications [31], but due to slow technology implementation in real consumer applications the AC based smart grid systems will be used in transition stage [86].

Micro-generation is a part of smart grid and distributed generation philosophy serving as a power source. It can be connected to distribution network nowadays or to AC based smart grid in near future. Micro generator includes all interface units and operates in parallel with the distribution network. Current rating of such devices is limited up to 16 A per phase [7]. Some energy sources can be connected directly to the distribution network, but in the case of DC power sources or PMSG based variable speed wind turbine (VSWT) systems it is necessary to use a power converter that interfaces the source and the AC grid.

VSWT based micro generators consist of a wind turbine, a generator and an interface converter (Fig. 0.4). Wind turbines capture wind energy and convert it to rotational mechanical energy. The generator converts mechanical energy into electricity, but the interfacing converter rectifies the input AC with variable voltage and frequency, adjusts voltage levels and inverts DC voltage into AC with grid voltage and frequency. The main objective of this dissertation is to develop a power part of an interface converter for PMSG based VSWT with power level up to 11kW that can be used as micro generator after control and user interface development.

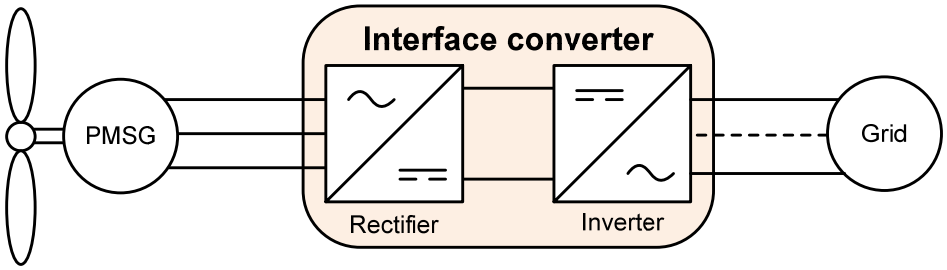


Fig. 0.4. General block diagram of WTS

1. CHALLENGES OF PMSG BASED WIND TURBINE

This chapter is devoted to definition of requirements and operation modes of converter for micro and small wind turbines in context of micro-generator and already developed converter analysis. The development of well suited converter for wind applications requires understanding of wind turbine generator system (WTGS) characteristics. Wind properties directly affect WTGS characteristics and for this reasons wind theory and wind regime is discussed in section 1.1. Since micro-generator can be connected to low voltage distribution or residential network, the main requirements and grid parameters are stated in section 1.3, but PMSG based WSVT characteristics are described in 1.3. The description and analysis of traditional grid tied converter topologies are given in section 1.5.

1.1. Wind energy conversion

Understanding of wind energy conversion principles and wind distribution is the basic for optimal converter development and its optimization. For this reasons wind energy conversion principles are described in this section.

1.1.1. Wind power conversion

Wind is a kind of air flow and, since this air has its own mass and speed, the wind contains some kinetic energy, which can be extracted. This energy is usually captured by an electromechanical generator which consists of wind turbine, some electrical generator and power electronic converter. Wind turbine transfers the energy from the air flow to the generator, where electrical energy is generated, but converter provides control of generator and turbine. The power contained in the wind passing a certain area with velocity is described by formula:

$$P_m = \frac{1}{2}\rho A v^3 \tag{1}$$

where A - swept area (m^2);

ρ - air density (kg/m^3);

v - wind velocity (m/s).

The air density depends on air pressure and moisture, but for practical calculations its value may be assumed as 1.2 kg/m^3. Only a part of the total wind power can be captured. The

amount of useful power in wind is described by power coefficient *Cp* and introducing it in (1) the amount of mechanical power captured by the turbine could be calculated:

$$P_{turbine} = \frac{1}{2} C_p \rho A v^3 , \tag{2}$$

where C_p - power coefficient of wind turbine.

The theoretic maximum value of power coefficient is 0.59 and it is called the Betz limit, but the maximum values lies between 0.4 and 0.5 for industrial wind turbines. Power coefficient is a function of the tip speed ratio (TSR) λ which is another important parameter for wind turbines. An example of power coefficient as function of TSR is shown in Fig. 1.1.

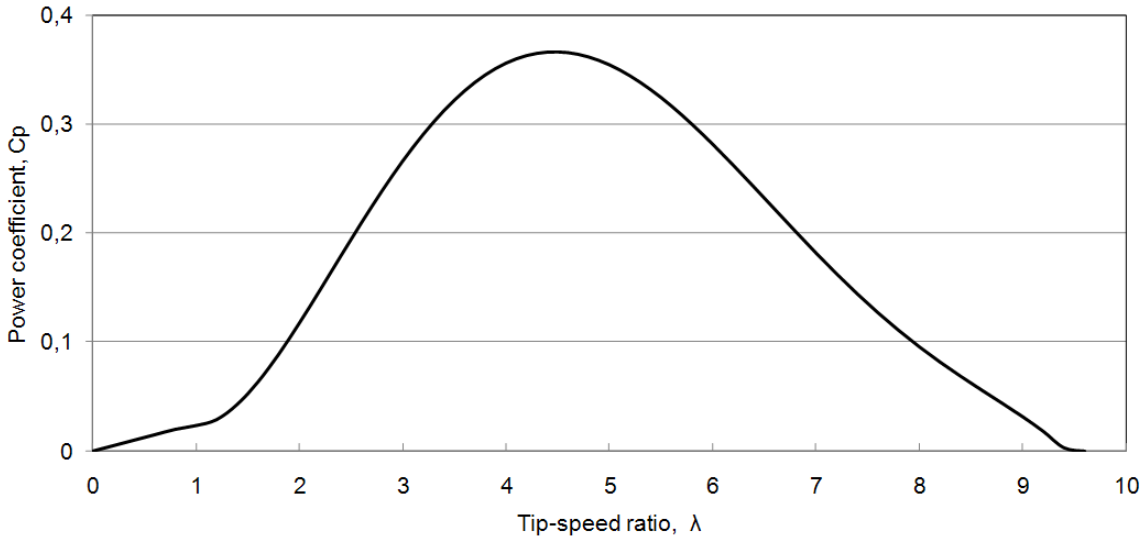


Fig. 1.1. Power coefficient C_p versus tip-speed ratio

The TSR shows the relation between circumferential velocity of the blade tips and the wind velocity:

$$\lambda = \frac{v_t}{v} = \frac{r\omega}{v} , \tag{3}$$

where r - radius of the wind turbine rotor (m);

v_t - velocity of the blade tip (m/s);

ω - angular rotor speed (rad/s).

As can be seen from Fig. 1.1, the power coefficient changes from zero to its maximum value and then back to zero with TSR change. It means that power coefficient have its maximum at certain TSR value λ_{opt}. Optimum value of TSR depends on turbine aerodynamics and type, for example: λ_{opt}=5...8 for three blade horizontal axis turbines and 4 to 7 for vertical axis designs [35]. Since the optimum value of TRS is constant for certain turbine, then

rotation speed of turbine should follow wind speed to obtain maximum mechanical efficiency. This aspect directly leads to variable speed operation of wind turbine to get maximum energy from wind. Wind mills with variable speed operation mode are named - variable speed wind turbines (VSWT).

Nominal rotation speed of turbines is affected by their size. Bigger turbines have longer blades and lower rotation speed to obtain optimum TSR. Rated rotation speed of small turbines with rotor diameter less than 2 meters is 500 rpm, usually, but big ones with 126 m rotor only 12.6 rpm. It shows that wind mills are slow running machines and multipole generators are required to eliminate the gear box [47, 94]. The PMSG are often utilized in such applications (Fig. 0.2).

1.1.2. Wind velocity distribution

The wind velocity determines the rotational speed of the VSWT and the generator. Since it has direct impact on power converter operation modes, an example of wind velocity distribution at 10 meter height is shown in Fig. 1.2, but the corresponding energy yield in Fig. 1.3. An average velocity is 5.4 m/s for these distributions. These distributions are obtained in the analysis of Pavilosta weather forecast data for the year 2009.

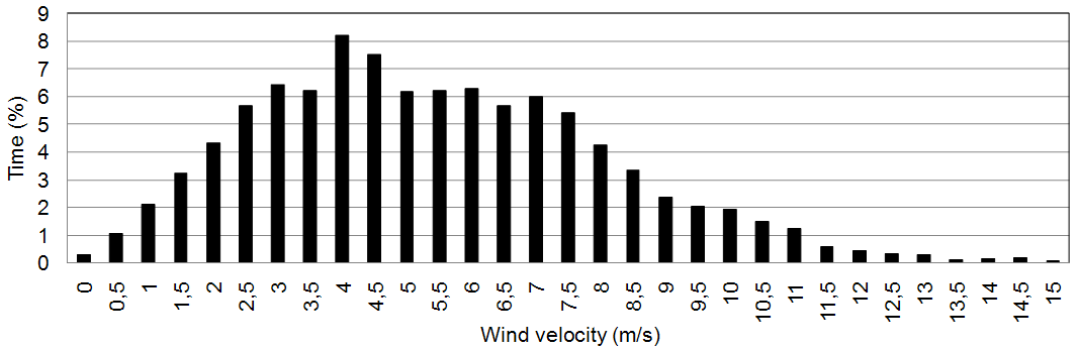


Fig. 1.2. An example of wind velocity distribution

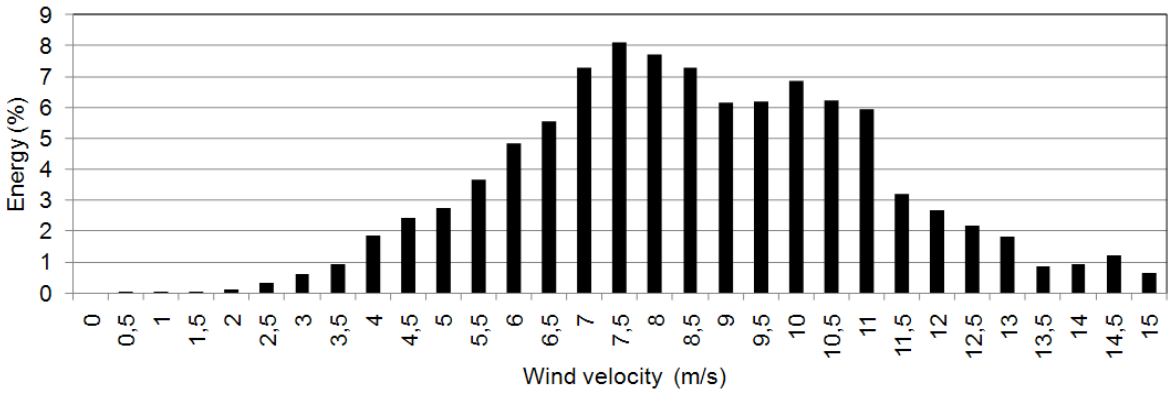


Fig. 1.3. An example of normalized energy yield

If only annual average value of wind velocity is available, then wind velocity distribution can be approximated by Reyleigh-distribution [35]:

$$t_r = \frac{\pi \Delta v}{2 v_{av}} \varepsilon \cdot \exp(-\frac{\pi}{4} \varepsilon^2), \text{ where } \varepsilon = \frac{v}{v_{av}}, \tag{4}$$

where t_r - relative time;

Δv - velocity step (m/s);

v_{av} - average wind velocity (m/s).

The Rayleigh distribution is the isolated case of the Weibull function with shape parameter equal to 2. The advantage of the Rayleigh distribution is that it only depends on the mean wind speed. Reyleight-distribution with v_{av}=5.4 are shown in Fig. 1.4. Wind velocity distribution approximated by Weibull-function. It can be seen that wind velocity distribution are quiet similar with statistical one in Fig. 1.2. and can be used for converter optimization purposes if more accurate data is not available.

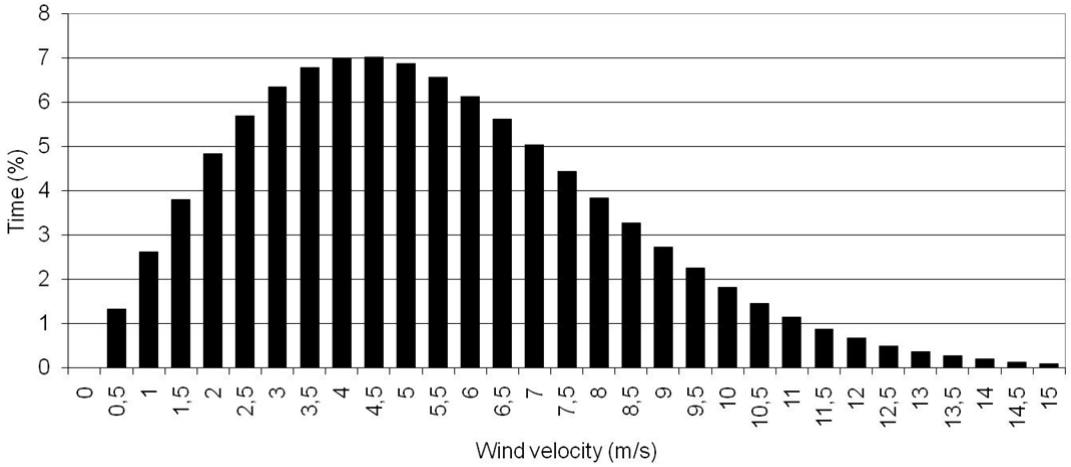


Fig. 1.4. Wind velocity distribution approximated by Weibull-function

Such average wind speeds are characteristic of Baltic coastal regions and so can be used as reference for interface converter design. Fig. 1.5 illustrates the average wind speeds in Baltic countries at 50 m height [11]. These values are more useful for commercial applications due to similar height of mast. Since the masts of small turbines are shorter – around 20 m, the average wind speeds are significantly lower. The average wind speed v_2 at height z_2 can be calculated from a reference speed v_1 at z_1

$$v_2(z_2) = v_1 \frac{\ln(z_2/z_0)}{\ln(z_1/z_0)}, \tag{5}$$

where z_0 - roughness length dependent on country (0.03 m – farmland; 0.1 m – trees; 0.5 – 1.6 m – forests) [35].

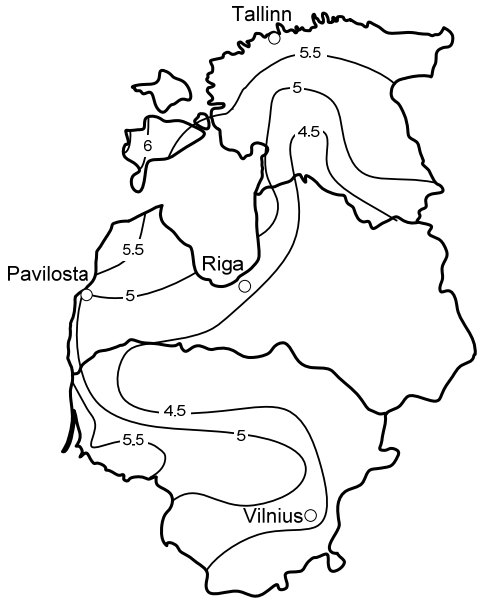


Fig. 1.5. Average annual wind speed in Baltic countries at 50 m height above terrain

Fig. 1.6. illustrates an example of the average wind speed change above the terrain. The reference speed is 5.4 m/s at 10 m height in this example. As one can see the average wind speed changes significantly with height and higher mast expenses should be evaluated before the turbine installation.

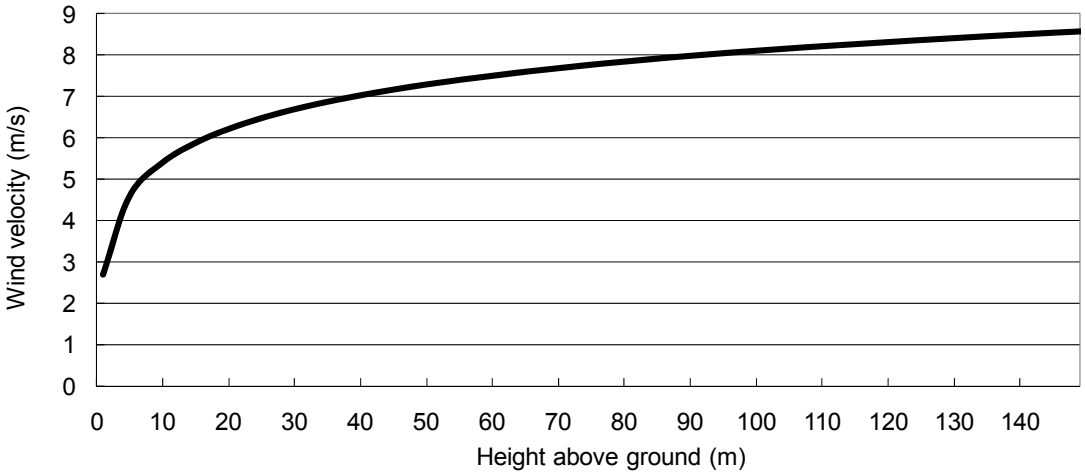


Fig. 1.6. Wind speed change above ground

1.2. WTS power configurations

The wind turbine system consists of two basic parts: a mechanical and an electrical one (Fig. 1.7.). Mechanical part of WTS extracts the energy from wind and makes the kinetic energy of air flow available to the generator shaft. The electrical part converts the electric energy from generator making it suitable for electric grid. The electric generator transforms the mechanical energy into electrical one and acts as the connection point of both parts of WTS [71].

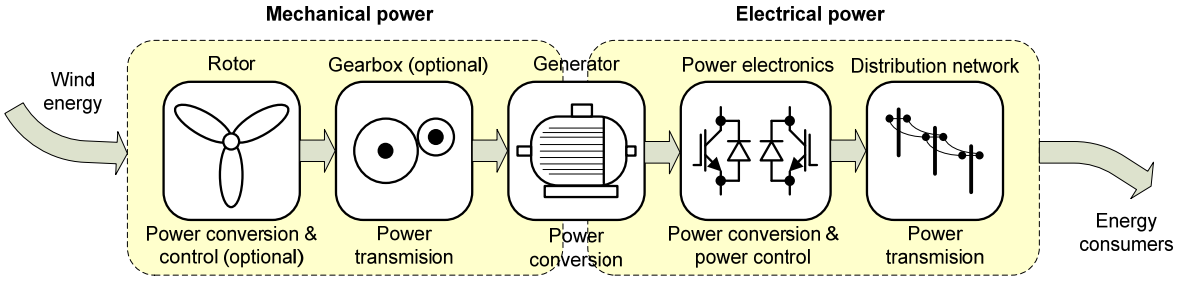


Fig. 1.7. Power conversion in wind turbine system

From WTS description one can see that there are three distinct stages that can be optimized for maximum wind energy extraction: mechanical, electromechanical and electrical. The mechanical stage may regulate the pitch angle of the blades, the yaw of the turbine shaft and the speed of generator shaft. The electromechanical stage can have different structures: different types of generators (synchronous, asynchronous and custom constructions [56]) with variable structure (pole pairs, excitation types) and some power converter for control of generator excitation. An electrical stage can have power electronics converter that adapts the grid and the generator voltages and controls the active and reactive power flows [10].

The power conversion structures of WTS discussed in literature [16], [34], [13], [100] and used in commercial applications [30] are illustrated in Fig. 1.8. The possible converter structure for the PMSG based small WTS are shown with colour boxes (Fig. 1.8.) [7], [9].

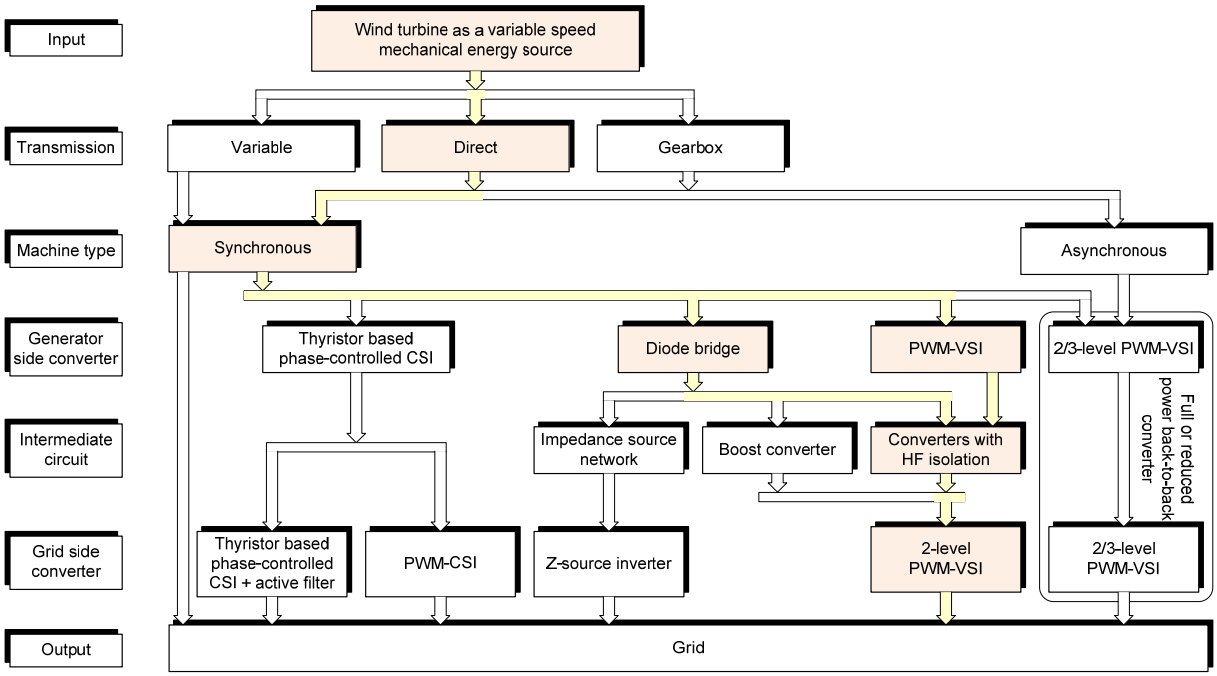


Fig. 1.8. Power conversion structures for variable-speed wind turbine system

1.2.1. Interface converter topologies for PMSG based VSWT

There are several topologies of interface converters for PMSG based VSWT studied in literature. They can be divided in topologies without isolation and ones with galvanic isolation by means of HF transformer utilisation. The general description of interface converters is given in this chapter.

One of the simplest transformerless interface converter topologies consists of uncontrolled rectifier and grid side converter (Fig. 1.9.). This topology is the cheapest solution due to low number of controlled switches and simple control system which is necessary only for the grid side inverter. The main disadvantage of this solution is the absence of DC link voltage regulation possibility that leads to lack of extracted power at low speeds [44]. Additionally, this topology does not offer any generator power and speed control possibilities that exclude MPPT functionality. All these disadvantages make this topology unsuitable for VSWT applications.

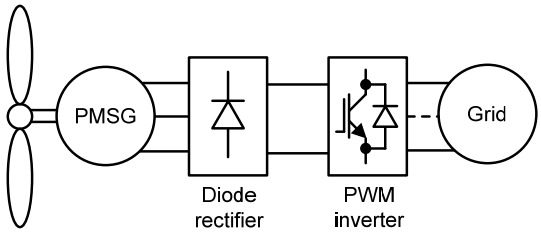


Fig. 1.9. Interface converter with a diode rectifier

` The topology with an additional boost converter (Fig. 1.10.) was introduced to improve the generator power control capability by keeping the power circuit of the converter at a simple level [24]. This topology offers a possibility to extract power at low wind speeds and thus significantly expand the operation range of the PMSG based VSWT system. These improvements are significant, but due to the limited PFC capability and lower efficiency than with a controlled rectifier, it is not feasible to use this topology with a boost converter in high efficiency applications [44].

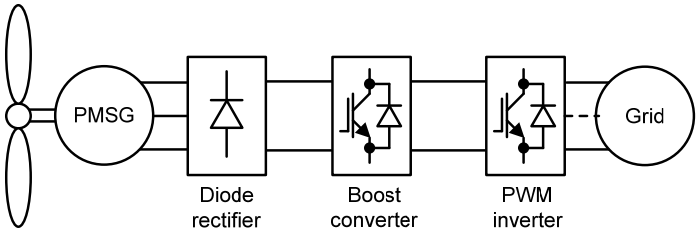


Fig. 1.10. Interface converter with an additional boost converter

The back-to-back converter (Fig. 1.11.) has high control flexibility of a generator torque and current [100]. Implementation of the controlled rectifier allows the generator to operate with the unity power factor and easily implement MPPT functionality.

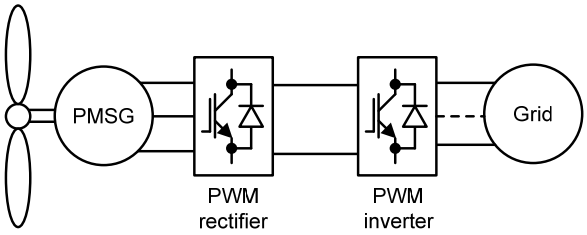


Fig. 1.11. Traditional back-to-back interface converter

The energy storage devices like batteries (Fig. 1.12.) can be added to the intermediate DC link of the back-to-back converter to improve the low voltage ride-through (LVRT) capability. The LVRT capability becomes more and more important in the context of grid code requirements [54]. The main disadvantage of the classical back-to-back converter is only two voltage regulation freedoms of the generator and grid side converters. The generator side converter can boost the generator voltage to obtain the necessary level of the DC link voltage, but the inverter can only reduce it.

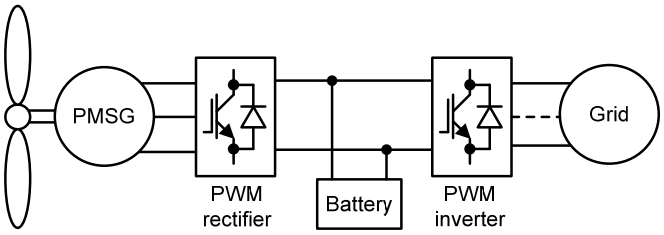


Fig. 1.12. Back-to-back interface converter with auxiliary battery for energy storage

Since the VSWT operates at low rotation speeds more than half a time [7] and the output voltage of the generator is significantly lower than the nominal at this mode, the boost properties of the interface converter become an issue. This is especially topical at micro power level, where the nominal generator voltage is lower than the grid voltage.

Implementation of Z-source inverters (ZSI) has become popular in recent years in applications where additional voltage boost is necessary [17]. The ZSI topology features the PWM inverter coupled with a symmetrical lattice network consisting of two inductors and two capacitors connected in X-shape (Fig. 1.13.). The ZSI has inherent voltage boost and buck capability using the shoot-through switching states in each phase leg of the PWM inverter. This enables the wind generation system to achieve the demanded variable-speed operation.

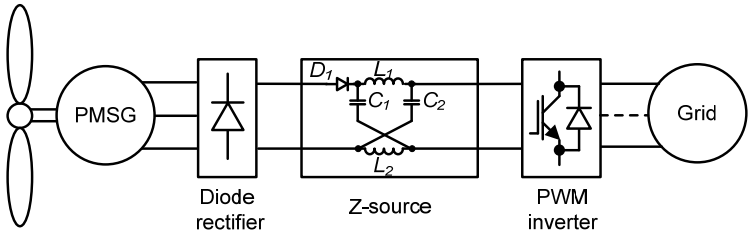


Fig. 1.13. Z-source network based back-to-back interface converter

Converters with HF isolation (Fig. 1.14.) represent the interface converter group mainly addressed for WTS connected to the residential power grids or systems connected to DC bus. (smart grid applications, for example). Interfacing converters with HF isolation are the main topic of this research.

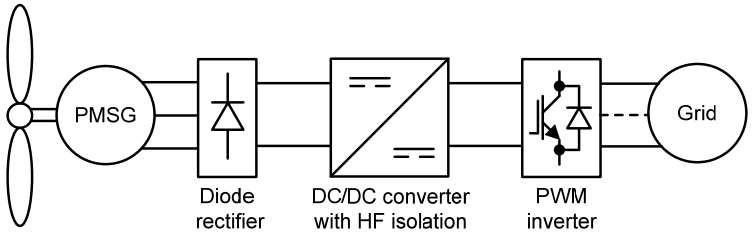


Fig. 1.14. Interface converter with a HF isolation

1.3. Residential network

Small wind turbine systems are usually utilised at rural and residential houses and are connected to residential power network. These networks are low voltage part of distribution network (Fig. 1.15.). Residential power networks utilize 400 V line to line voltage or 230 V phase to neutral voltage. These voltages can vary depending on load conditions and distance from substation. Voltage tolerances for the residential networks are defined by the standard EN 50610. The general requirements from EN 50160 are summarised in Table 1.1 [67], but harmonic content allowed in Table 1.2. The interface converter should be able to transfer the power from wind turbine to grid at all power network operation conditions predefined by the standard requirements. It means that output voltage of converter should be higher than nominal at least by 15% or reach the 265 V value for one phase system [55].

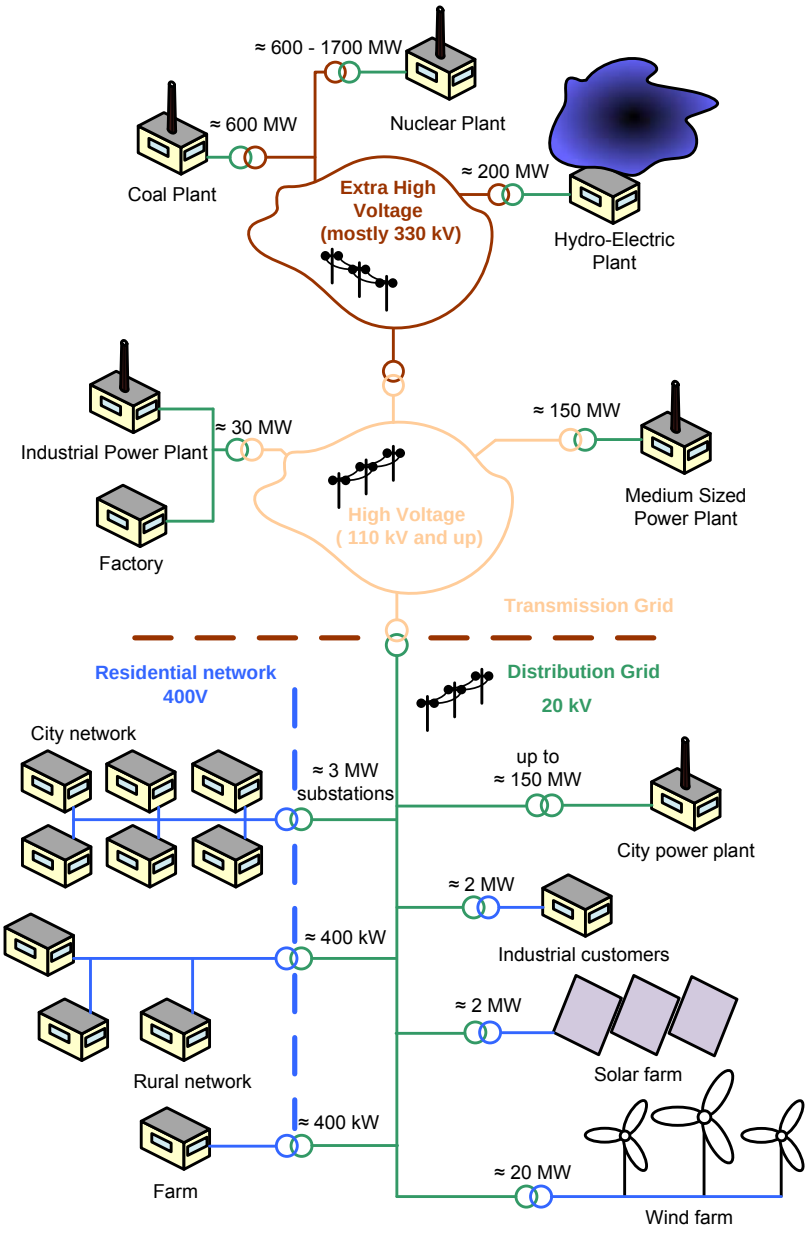


Fig. 1.15. The structure of utility grid

Table 1.1

General voltage characteristics of LV public distribution system

No	Parameter	Description	Supply voltage characteristics according to EN 50160
1	Power frequency	Mean value of fundamental measured over 10s	±1% (49.5-50.5 Hz) for 99.5% week - 6% / +4% (47-52 Hz) for 100% week
2	Voltage magnitude variations	Mean value of fundamental RMS value over 10 minutes	±10% for 95% of week
3	Rapid voltage changes	Normal: Infrequently:	5% 10%

Table 1.2

Values of individual harmonic voltages at the supply terminals in percent of U_n

Odd harmonics				Even harmonics	
Not multiples of 3		Multiples of 3			
Order h	Relative voltage (%)	Order h	Relative voltage (%)	Order h	Relative voltage (%)
5	6	3	5	2	2
7	5	9	1.5	4	1
11	3.5	15	0.5	6…24	0.5
13	3	21	0.5		
17	2				
19	1.5				
23	1.5				
25	1.5				

1.4. PMSG based WSVT characteristics

Utilization of PMSG in VSWT applications becomes more and more popular during last decades [4] especially at micro and small power WTS. The popularity of the PMSG usage is determined by three features: high efficiency, possibility of multipole design implementation and maintenance free operation. High efficiency is obtained by utilization of permanent magnets that eliminates excitation loses in the generator. The utilization of multipole PMSG offers slow speed operation and the possibility of gearless WTS construction. The operation of PMSG does not require frequent maintenance since there are no brushes. Only bearing is the thing which can wear out. Despite the many advantages of PMSG there are some major drawbacks.

The main drawback of PMSG is the dependence of its output voltage on the rotation speed. The difference between the minimum and the maximum voltage can reach four times in VSWT applications [70]. This drawback can be easily overcome with the help of an appropriate interfacing converter. Another drawback is high weight and price of multipole PMSG that leads to utilisation of fast running machines together with gearbox for large scale turbines [28]. The 8 pole PMSG generator with 1.2 kW power was used as power source in this research. The main parameters of the generator are collected in

. The generator was driven by asynchronous motor with belt transmission (Fig. 1.16.). The motor speed was controlled by ABB frequency converter to imitate the wind turbine speed change and obtain all operation modes of VSWT.

Table 1.3

Parameters of PMSG

Nominal power	1160 W
Nominal current	5 A
Nominal voltage	134 V
Nominal speed	375 rmp
Phase resistance	1.2 Ω
Phase inductance	5 mH
Number of pole pairs	8

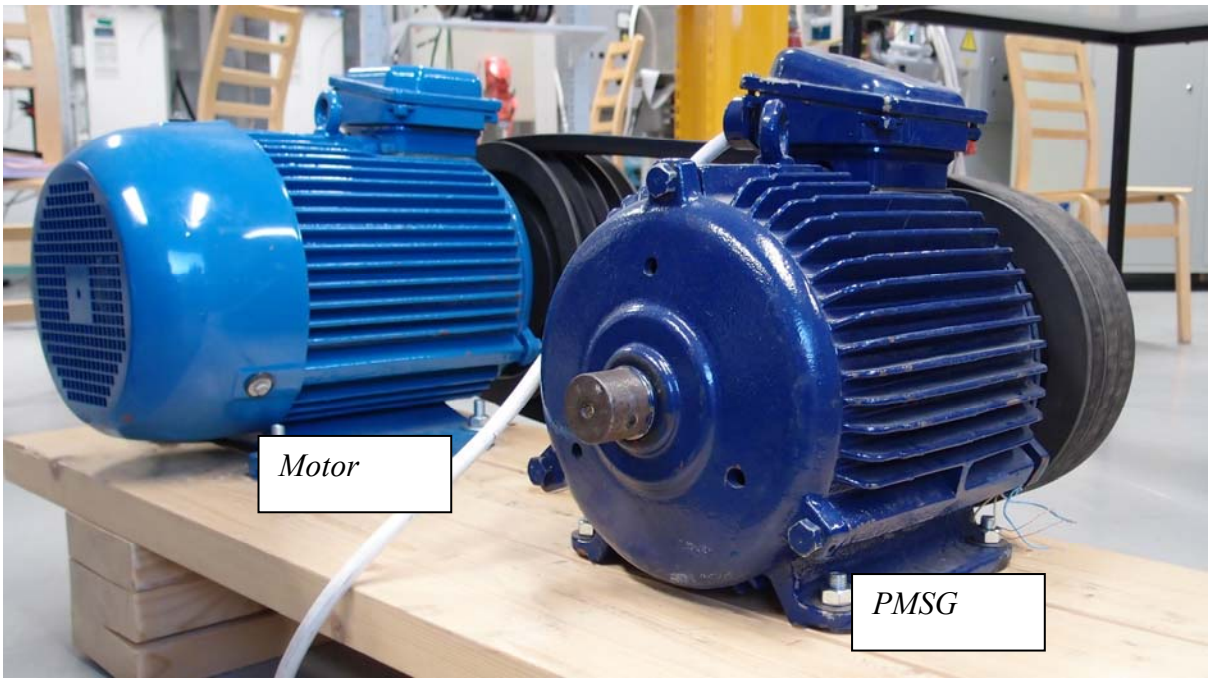


Fig. 1.16. Experimental stand for PMSG tests

VSWTs have three distinct operation modes: silent mode, variable speed operation mode and constant speed mode. A turbine is silent in two cases: wind speed is below a cut-in level or above the cut-off speed. If the speed is below its cut-in level it produces insufficient torque to move the turbine. At the same time winds above the cut-off level may damage the turbine that must be stopped at such conditions. A turbine usually starts to operate at 3.5 m/s and it should be stopped at the wind speed above 25 m/s [35]. Turbines operate at variable speed in the wind velocity range from cut-in to rated wind speed. Rated wind speed differs by turbine types, but often has the value of 12 meters per second. The turbine has rated output power at rated wind speed. Constant speed mode takes place above the rated wind speed. The output power of turbine remains constant at this mode. Fig. 1.17. illustrates the maximal power curve of the example wind turbine with rotor diameter of two meters that match to our PMSG.

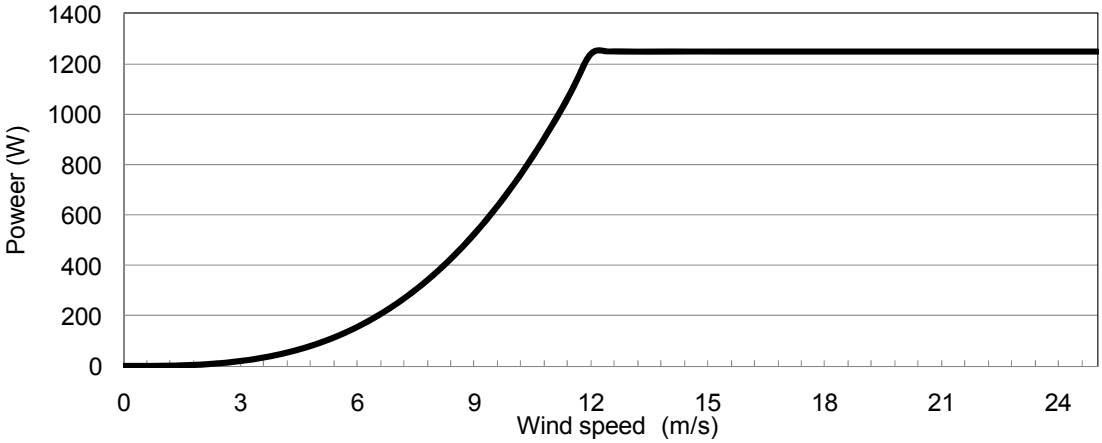


Fig. 1.17. Output power of PMSG based VSWT

The turbine power dependence on its rotation speed at fixed wind speeds is illustrated in Fig. 1.18. One can see that the maximal power can be captured from wind turbines only if they are of a variable speed type. It means that generator's speed is four times lower at the cut-in wind velocity than at the rated conditions to capture maximal power at all usable wind velocity range. Since the turbine power depends on the generator rotation speed and wind speed ratio the maximum power point tracing algorithms should be used for interface converter control [16].

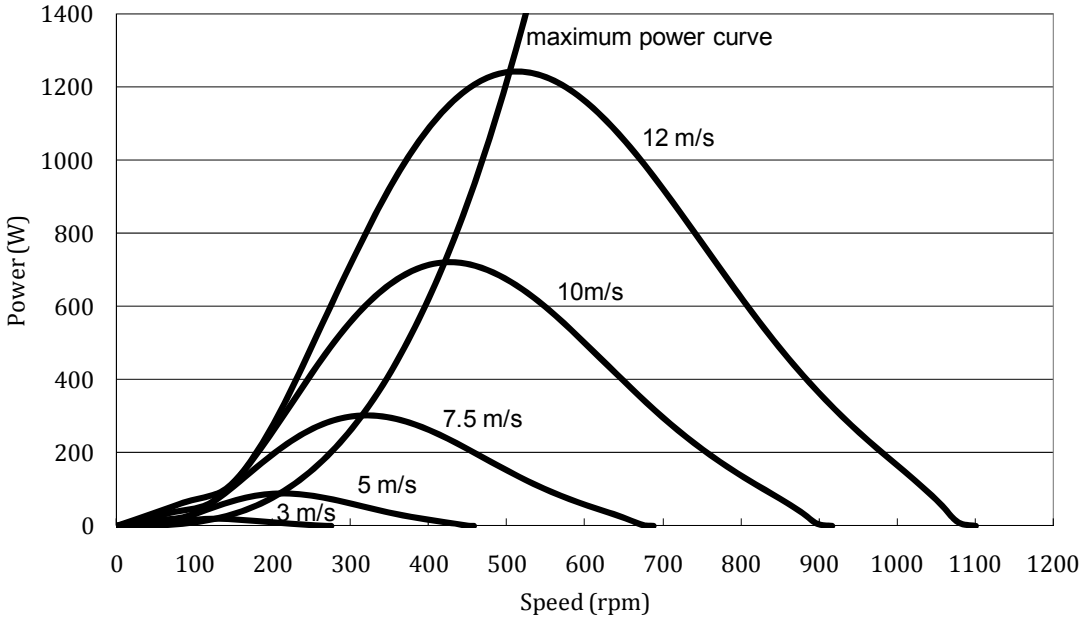


Fig. 1.18. VSWT power vs. rotation speed of turbine at different wind velocities

The rotation speed dependence on wind velocity of the generator and its voltage characteristics is illustrated in Fig. 1.19. It clearly demonstrates the wide range of generators output voltage and wind turbine operation modes.

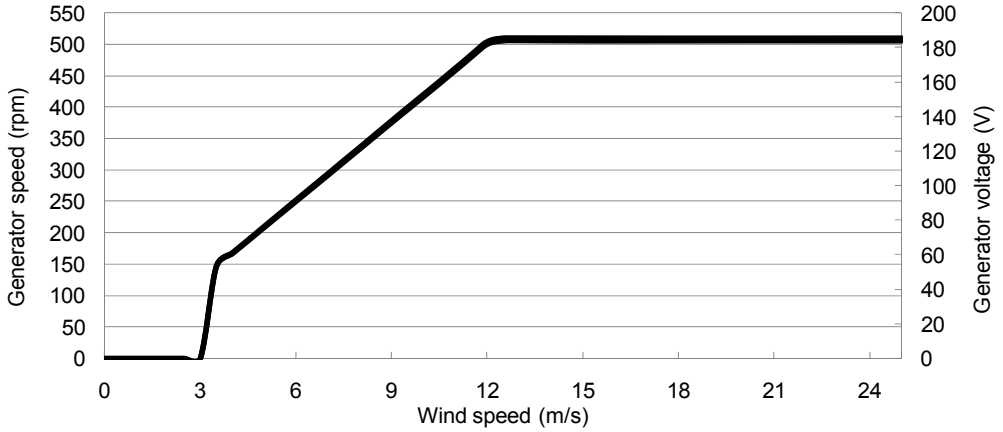


Fig. 1.19. Generator speed and voltage vs. wind speed

The generator operation modes (Table 1.4) were defined depending on its rotation speed and turbines captured energy. The rated speed corresponds to wind speed with maximum captured energy (Fig. 1.3.) and are close to nominal speed of generator. Generator will operate at slow speed mode 46 % of time, but captures only 22 % of total energy. Only 17 % of time the generator will operated at rated speed mode and will capture 27 % of energy, but 51 % of energy can be captured at high speed mode spending only 12 % of time. Such energy and corresponding time distribution indicates that energy produced by wind turbine can be fully utilized together with utility power supply. This is the reason for popularity of grid connected or grid-tied systems and the main reason for research in this field. Such distribution of wind energy illustrates another feature of wind power utilization that should be considered in interface converter design: converter operates at partial loads for long. It means that converter efficiency should be high at wide power range to improve the base load energy demand satisfaction. There are no any other opportunities for wind energy since its unpredictable nature.

Table 1.4

Generator operation modes

	No speed	Slow speed	Rated speed	High speed
Wind velocity range	0 – 3 m/s	3.5 – 6.5 m/s	7 – 8.5 m/s	9 – 25 m/s
Operation time at this mode	25 %	46%	17%	12%
Captured energy at this mode	0%	22%	27%	51%
Power range at this mode	0%	3 – 16 %	16 – 35 %	35 – 100 %
Generator speed	0	147 – 273 rpm	273 – 357 rpm	357 – 510 rpm

1.5. Topology analysis of interface converters for WSVT

There are a lot of interface converter topologies without galvanic isolation studied in literature, but only few researches are devoted to topologies with high frequency isolation for micro and small wind applications [16,32,34]. In [16] the authors have proposed a buck type isolated DC/DC converter (Fig. 1.20).

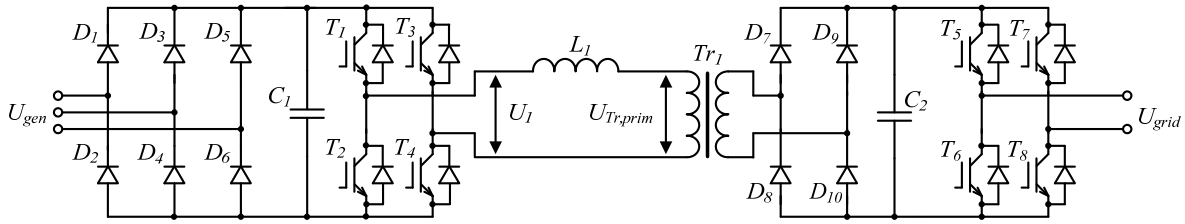


Fig. 1.20. Buck type isolated DC/DC converter

Variable generator voltage is rectified with a three-phase diode bridge firstly into proportional DC voltage. Stabilization of the second DC link voltage is obtained with the buck type isolated DC/DC converter by means of duty cycle variation. The main drawback of buck type converter utilization in wind applications is high currents in the transformer's primary winding and HF inverter switching devices at rated wind speeds. Moreover such topology does not offer possibility to use low voltage transistors: they should withstand the maximal voltage of the first DC link voltage U_{C1} (Fig. 1.21.). Fig. 1.21. illustrates the simulation results of buck type

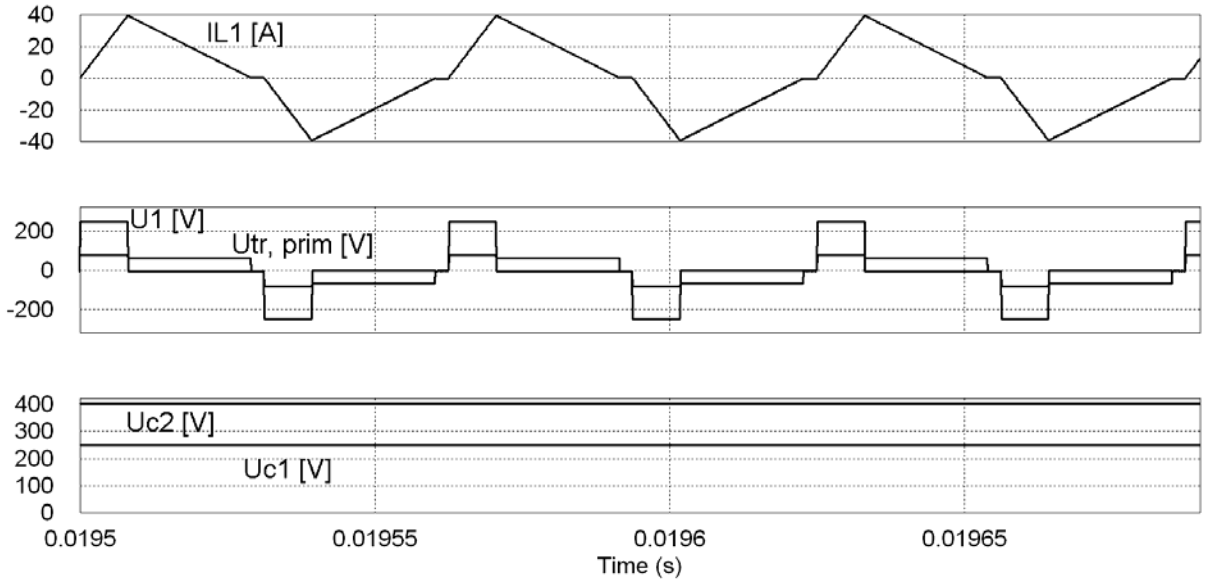


Fig. 1.21. The main current and voltage waveforms of buck type isolated DC/DC interface converter at 1250W load

interface converter at 1250W load. One can see that inductor current I_{L1} is enormous for 1.3kW converter and will lead to high power losses is HF inverter switches, inductor and transformer primary windings. On the other hand there will be high switching losses at cut-in conditions due to high power transistor utilization in HF inverter. The inductor current I_{L1}, HF inverter output voltage U_1 and transformer primary voltage $U_{Tr,\,prim}$ and both DC link voltage U_{C1}, U_{C2} waveforms of buck type interface converter at 40W load are demonstrated in Fig. 1.22. Previously mentioned disadvantages make this topology unattractive for wind applications.

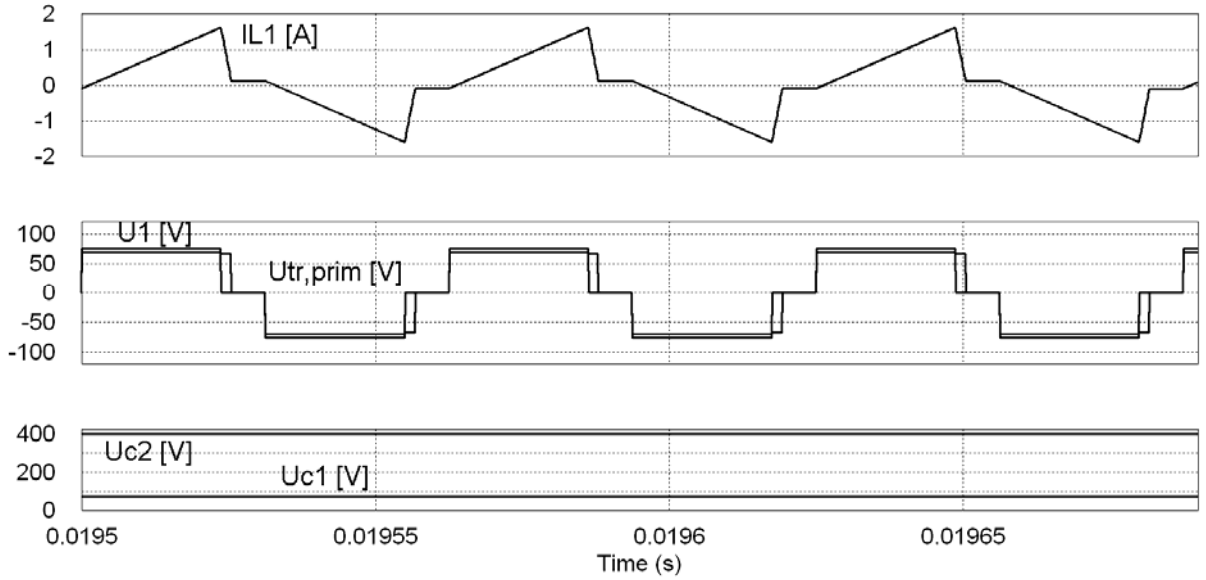


Fig. 1.22. The main current and voltage waveforms of buck type isolated DC/DC interface converter at 40W load

In [34] the authors have proposed a one-phase soft-switched dual LCL DC/AC converter (Fig. 1.23). This converter utilizes a controlled rectifier for generator voltage rectification and DC link voltage stabilization. The generator side DC link is connected with

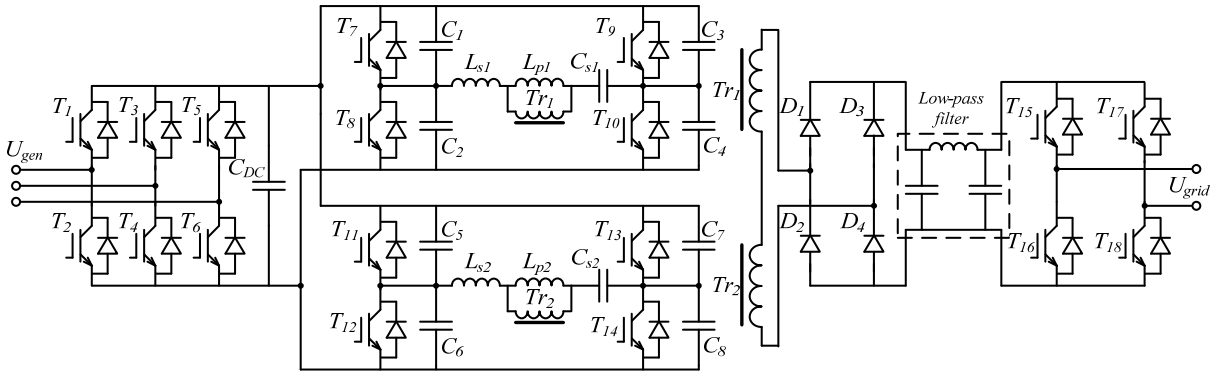


Fig. 1.23. A HF isolated dual-bridge LCL resonant converter

two HF LCL resonant inverters connected in parallel. The secondary side of HF transformers are connected in series for better voltage regulation capabilities. The output voltage of series connected HF transformers is rectified into DC voltage with diode bride. This rectified voltage (HF transformer output voltage too) contains ripple with grid frequency. In such way it is possible to reduce the switching frequency of grid side inverter. This pulsating voltage is filtered by low pass LCL filter to remove the high frequency component and after is inverted with line connected inverter (LCI) The switches of LCI is commutated when line voltage cross the zero point. High switching frequency of the HF inverter (100 kHz) helps to reduce the low pass LCL filter size, but low switching frequency of LCI eliminates the switching loss in this converter part.

The main disadvantage of dual-bridge LCL resonant converter is big amount of controlled switches (Table 1.5) that needs driver circuits and appropriate control unit. Another disadvantage is reported efficiency of proposed converter prototype: only 90 % at 500 W (nominal load) and 83 % at 250 W load [85]. Reduced efficiency at partial load will significantly reduce the total energy transmitted to the grid that can be the worst case for wind turbine applications.

Analysis of two topologies with HF isolation studied in literature for VSWT applications shows the significant disadvantages in terms of efficiency issues and complexity. Buck type isolated interface converter has relative simple circuit, but high current stress on semiconductor devices in HF inverter and primary winding of transformer can lead to big converter size and high price. Dual bride LCL resonant converter offer soft switching approach at HF isolation and LCI stages, but still has high circuit complexity and low reported efficiency. For these reasons the new HF isolated converter topology for wind applications is proposed in next chapter.

Table 1.5

Component count in two reviewed topologies

Topology / Elements	Buck type converter	Dual bridge LCL resonant converter
Transistors	8	18
Diodes	10	4
Transformers	1	2
Inductors	1	2
Capacitors	2	3

1.6. Conclusions

Analysis of wind theory shows that maximal energy from wind can be captured by variable speed wind turbines. Variable speed operation leads to variable output voltage of PMSG that is the most widespread electric machines for mechanical energy conversion in electricity in micro and small scale wind turbine systems due to high efficiency and possibility of multipole design and following elimination of gearbox. The output voltage range of PMSG can reach 4 times VSWT and this is the main parameter for interface converter that should be taken into account at converter design. Another feature of wind energy is unpredictable nature and wide power range that should be transmitted from turbine to grid. This fact has high importance if wind velocity distribution is taken into account. It shows that converter will operate at partial loads most of the time and for this reason converter efficiency should be as high as possible at partial loading.

Due to voltage and power characteristics of the PMSG based VSWT an interface converter topology utilizing converters with boost properties seams the most suitable solution for this application.

2. NEW ISOLATED CONVERTER TOPOLOGY

To improve the overall performance of the PMSG based VSWT system a new converter topology is proposed in [8], and is presented in Fig. 2.1. It consists of a three-phase full bridge controlled rectifier (generator side inverter) with PFC functionality and a quasi-Z-source (qZS) DC/DC converter with an HF transformer for galvanic isolation. The HF voltage of transformer is rectified by voltage doubler rectifier. The full bridge inverter with LC filter is used for interface converter connection with grid.

The proposed interface converter utilizes the multistage energy conversion. First, the controlled rectifier converts the variable voltage with the variable frequency U_{gen} from the PMSG into a DC voltage U_{DC1}. The qZS DC/DC converter offers galvanic isolation and voltage level adjustment between the generator side and the grid side DC links. Utilization of a unique qZS network and appropriate control offers an additional voltage regulation freedom at high efficiency. In such a way both converters together are responsible for the stabilized grid side DC link voltage U_{DC2}. Stabilized DC link voltage U_{DC2} can be inverted into the grid current by an appropriate inverter. The modulated output voltage of the inverter is smoothed by output LC filter to obtain purely sinusoidal voltage U_{grid}.

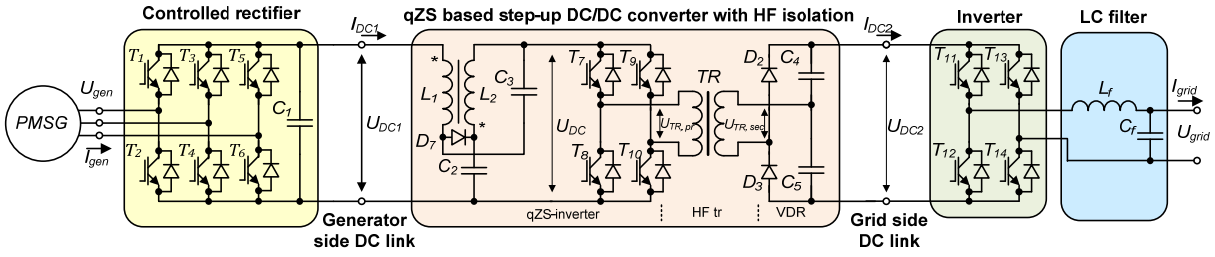


Fig. 2.1. Power circuit of proposed interface converter

Converter operation modes at different wind speeds for the particular application with 1.3 kW PMSG are illustrated in Fig. 2.2. It is seen that the demanded voltage boost could be obtained in two steps. First, the controlled rectifier stabilizes the generator side DC link voltage U_{DC1} to a 150 V level when the PMSG voltage is in the range between 45 V at cut-in conditions and below 112 V. The generator-side rectifier works as an uncontrolled rectifier when the PMSG voltage U_{gen} is above 112 V. In this mode the voltage U_{DC1} is changing proportionally to the PMSG voltage, from 150 V in the rated speed conditions up to 250 V near the cut-off point. After the rectifier, the qZS based step-up DC/DC converter finally stabilizes the grid side DC link voltage U_{DC2} at 400 V DC despite variations in the generator

side DC link voltage U_{DC1} in the range from 150 V to 250 V and also provides the demanded galvanic isolation.

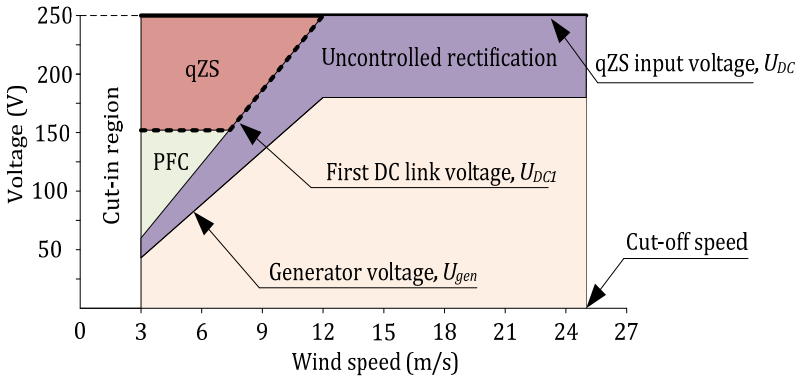


Fig. 2.2. General operation modes of the interface converter

In the following sections the main parts of the proposed interface converter are analyzed and discussed in more detail. The simulation results of lossless model of generator side converter and qZS DC/DC converter are shown to validate the proposed operation modes. The theoretical assumptions are experimentally validated by help of the 1.3 kW test setup (Fig. 2.3.) assembled in accordance with schematics presented in Fig. 2.1. The discussed application was powered with 1.3 kW PMSG with 8 pole pairs and the converters were tested separately.

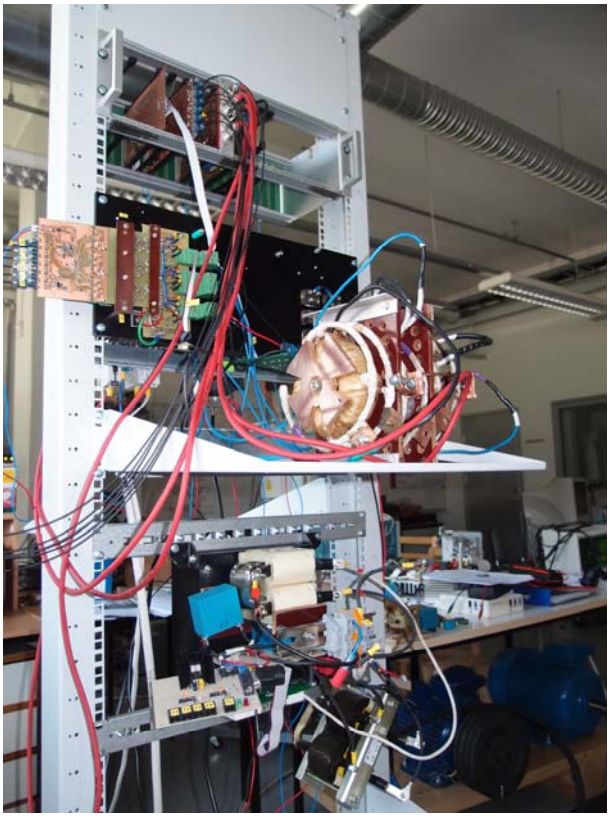


Fig. 2.3. Laboratory test setup of interface converter

A general specifications of experimental setup is collected in Table 2.1.

Table 2.1

General specifications of test setup

Component	*Value or type*
PMSG	
Phase resistance	1.2 Ω
Phase inductance	5 mH
Interface converter	
$T_1 \ldots T_6$	600 V/48 A IGBT (IXSH24N60AU1)
$T_7 \ldots T_{10}$	600 V/12 A IGBT (G4PC30UD)
D_1	600 V/120 A fast diode (STTH200L06TV)
D_2, D_3	1.2 kV /60 A FRED (DSEI2x61-12B)
Capacitance of C_1	470 uF
Inductance of L_1 and L_2	1.2 mH
Capacitance of C_2 and C_3	60 uF
HF transformer turns ratio	1: 1.2
Capacitance of C_4 and C_5	25 uF

2.1. Generator side converter

A three-phase PWM rectifier is used in the proposed interface converter to improve the PMSG current shape and ensure 150 V level of the generator-side DC link voltage at the lowest generator voltage. The equivalent circuit of the PMSG together with the three-phase controlled rectifier is shown in Fig. 2.4.

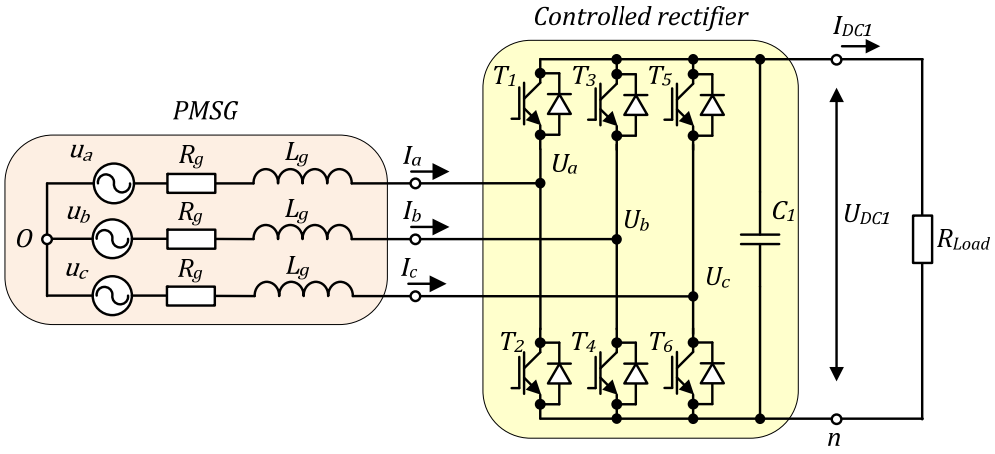


Fig. 2.4. Equivalent circuit of the PMSG and the controlled rectifier

The PMSG is substituted by the voltage sources u_a, u_b and u_c, phase resistances R_g and inductances L_g assuming that generator parameters are equal in all phases. The stator inductor of the PMSG serves as the boost inductor in this application. The first harmonic component of the PMSG voltage will be used for the PWM rectifier analysis.

Generator voltage equations are given by

$$\begin{aligned} u_a &= \hat{U}_a \sin(\omega t) \\ u_b &= \hat{U}_b \sin(\omega t - 120°) \\ u_c &= \hat{U}_c \sin(\omega t - 240°) \end{aligned} . \tag{6}$$

The phase shift between the generator's internal voltage sources and the output voltage is not taken into account due to the small inductance value.(7)

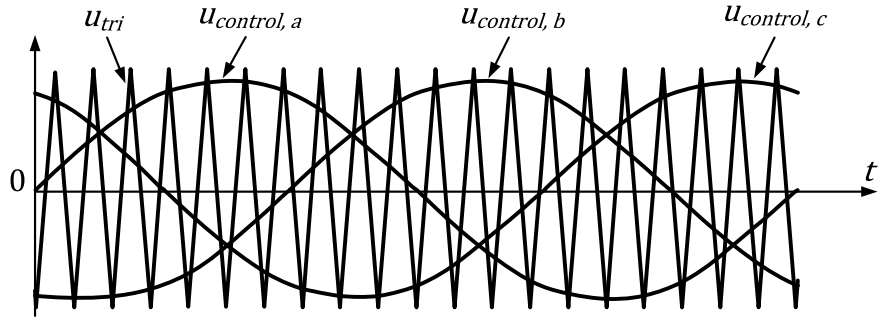
The transistor switching functions S1, S2, S3, S4, S5, S6 are defined as

$$\begin{aligned} S_1 &= \frac{1 + M \cdot \sin(\omega t)}{2}, & S_2 &= \frac{1 - M \cdot \sin(\omega t)}{2}, \\ S_3 &= \frac{1 + M \cdot \sin(\omega t - 120°)}{2}, & S_4 &= \frac{1 - M \cdot \sin(\omega t - 120°)}{2}, \\ S_5 &= \frac{1 + M \cdot \sin(\omega t - 240°)}{2}, & S_6 &= \frac{1 - M \cdot \sin(\omega t - 240°)}{2}, \end{aligned} \tag{7}$$

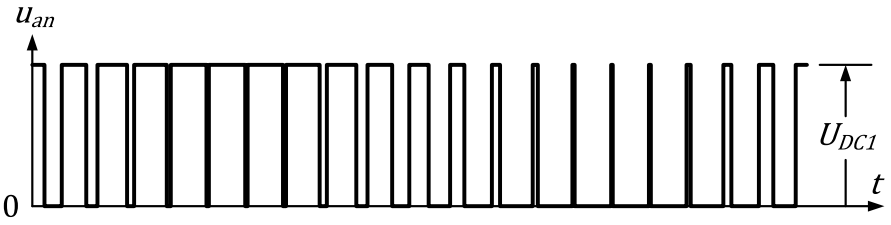
where M - is the modulation index that is defined as

$$M = \frac{\hat{U}_{control}}{\hat{U}_{tri}}. \tag{8}$$

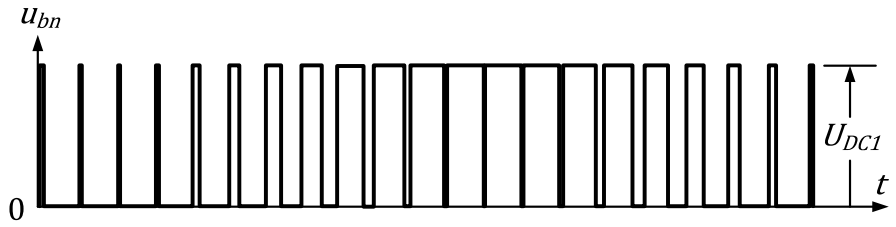
Applying the above switching functions to the corresponding transistors, the unipolar modulated voltages u_{an}, u_{bn} and u_{cn} can be seen (Fig. 2.5*b*, *c*, *d*) in the midpoint of the phase legs.



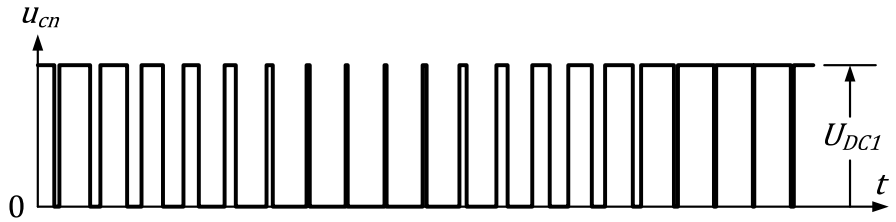
(a)



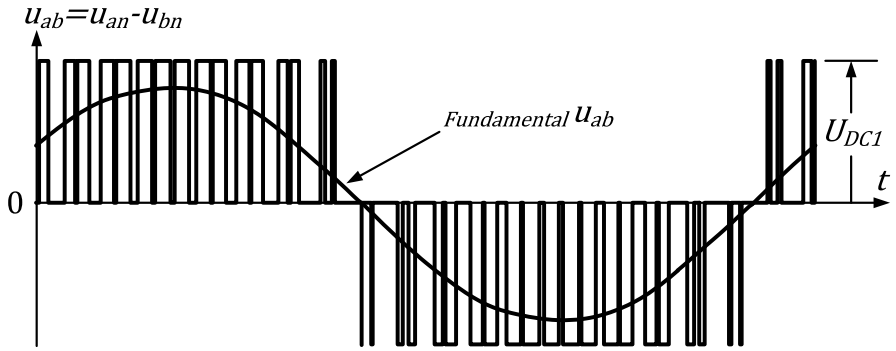
(b)



(c)



(d)



(e)

Fig. 2.5. Three-phase PWM voltage waveforms

The peak value of the fundamental frequency component of this voltage is

$$\hat{U}_{an} = M \frac{U_{DC1}}{2}. \tag{9}$$

Therefore the RMS value of the rectifier's line voltage is

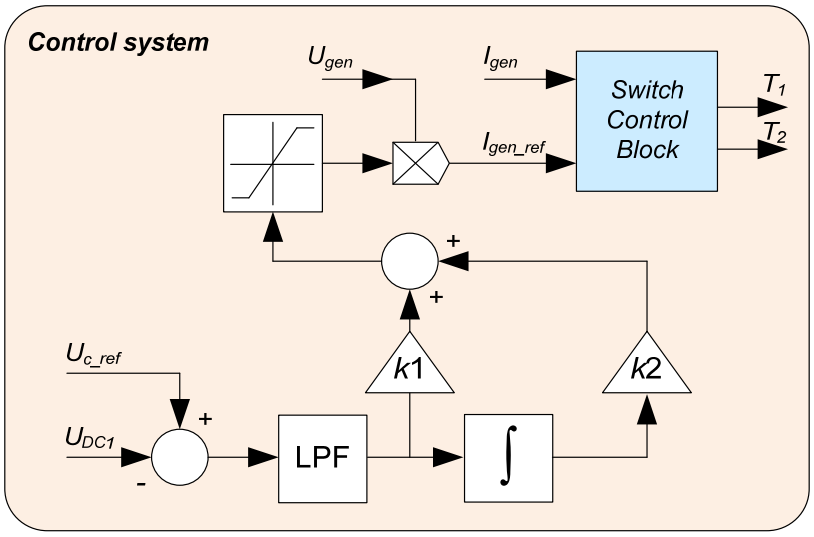
$$U_{ab} = \frac{\sqrt{3}}{\sqrt{2}} \hat{U}_{an} = \frac{\sqrt{3}}{2 \cdot \sqrt{2}} M \cdot U_{DC1}. \tag{10}$$

The ratio B_1 of the controlled rectifier input and the first DC link voltage can be expressed

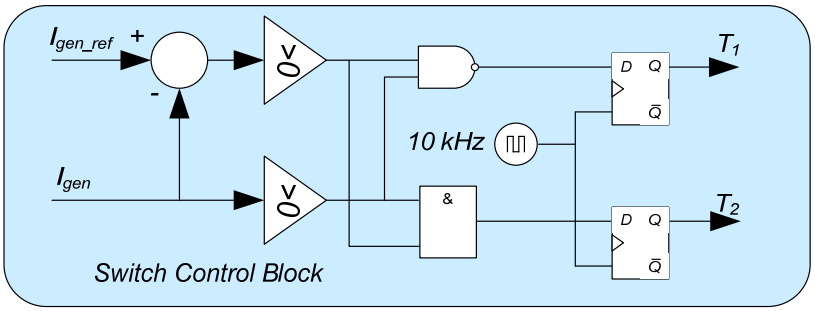
$$B_1 = \frac{U_{DC1}}{U_{ab}} = \frac{2 \cdot \sqrt{2}}{M \cdot \sqrt{3}} = \frac{1.633}{M}. \tag{11}$$

The waveform of the rectifier line voltage is shown in Fig. 2.5*e*. It is clearly seen that the output voltage of the controlled rectifier will be higher than the amplitude value of the generator line voltage U_{gen} even at the unity value of the modulation index. To obtain equal values of the generator side DC link voltage U_{DC1} and the amplitude value of the generator line voltage, the modulation index should be increased to 1.15. The transistor switching function is no more sinusoidal in this mode [59].

The control algorithm of generator side inverter is built according to the PWM method of control (Fig. 2.6*a*).



a)



b)

Fig. 2.6. Control system of generator side inverter (for one phase)

The input values of regulator enter the instantaneous value of generator side DC link voltage U_{DC1} and the reference voltage U_{C_ref} equal to the necessary voltage level. In order to escape pulsations of voltage across capacitors, only constant component of voltage is used. Further voltage error is feed to the PI regulator, whose output determines the amplitude of reference current. The form of reference current is determined by supply voltage, as a result

the current is in-phase to the voltage. Nonlinear element of the type “saturation” is used for limiting the amplitude of current. Further reference current will be given to the controller of the commutation of power switches. The unit of the commutation of power switches is built according to the method of vector control of power switches. In Fig. 2.6*b* the scheme of controller is represented.

Thus, transfer of the necessary active power to the load or generator side DC link is ensured. In the steady-state mode the value of error is equal to zero, value from the output of integrator is constant. In this case the power transferred to generator side DC link is equal to the output power of the generator.

The flowchart of the control algorithm (Fig. 2.7) clearly illustrates the control process of the generator side inverter.

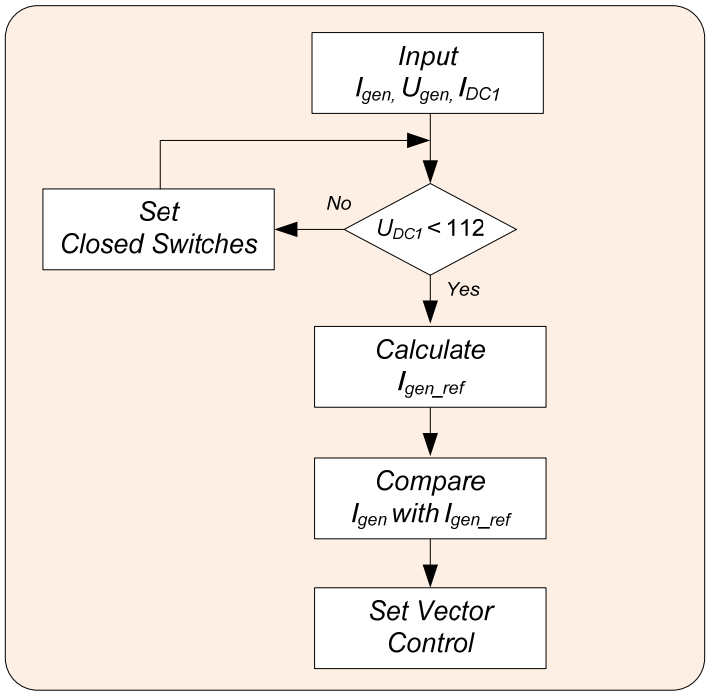


Fig. 2.7. Flowchart of the control algorithm for the generator side inverter

The controlled rectifier operates in the PFC mode and boosts the generator voltage to 150 V level when the line voltage of the generator is below the level of 112 V. The PFC signal generation is stopped and the uncontrolled rectification mode takes place, when the generator line voltage is higher than 112 V.

2.1.1. Simulation results of generator side inverter

In order to check chosen control algorithm simulation has been carried out. It should be noted, that scheme has been changed. The additional inductors were embedded after turbine. It allows to measure voltage shape from generator correctly and restricts current ripple. Also analog RLC filter is used to measure voltage shape from generator correctly

The first simulation was performed at the generator voltage U_{gen} = 53 V and 40 W load (Fig. 2.8.). At the time moment t=0.1 s, the regulator is switched on and the capacitor voltage level is gradually increased up to reference level 150 V. The amplitude of current is simultaneously raised up to the level that corresponds to the consumed power in this case. It is evident that current shape follows generation voltage. THD is about 31%. There are high frequency ripple that can be reduced by additional serial inductance or increased switching frequency of power switches.

The second simulation was performed at rated generator speed conditions, with the generator speed at 315 rpm and turbine power at 330 W. At this point the amplitude of the generator voltage U_{gen} is 150 V and boost control are not needed (Fig. 2.9). At the time moment t=0.1 s, the regulator is switched on. The generator current doesn't follow the voltage shape in this mode that can be considered as a disadvantage. Such situation is caused by relative low voltage difference between DC link and generator voltage. THD is improved from 41% to 31%.

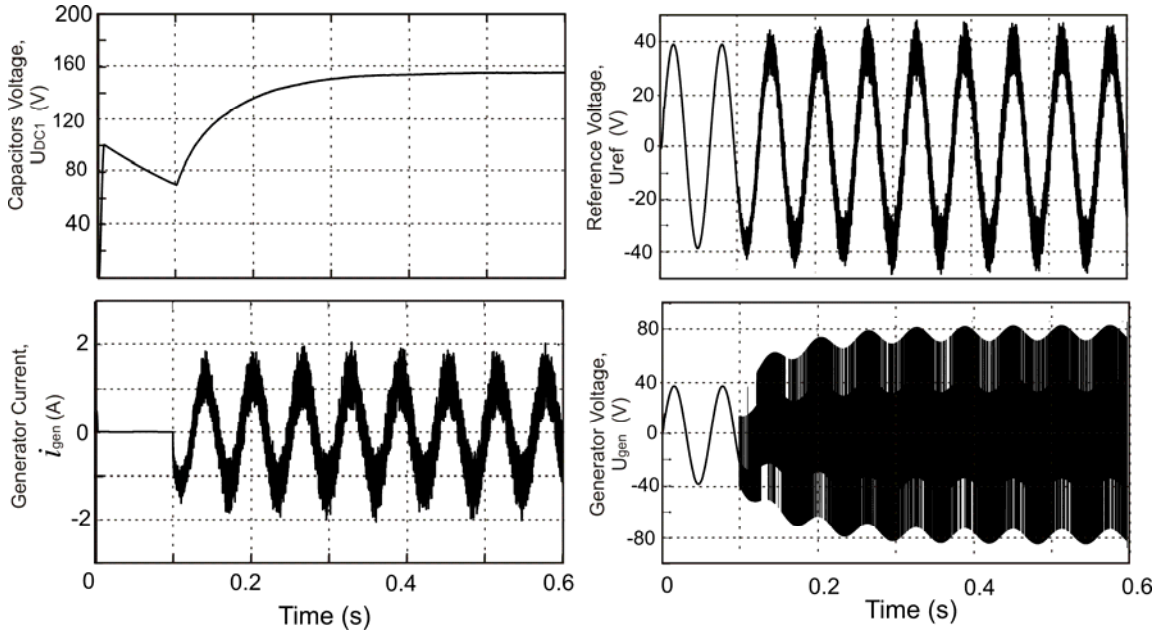


Fig. 2.8. Generator side DC link voltage U_{DC1}, PMSG current i_a, and voltage U_{gen} and filtered generator voltage U_{ref} at 40 W

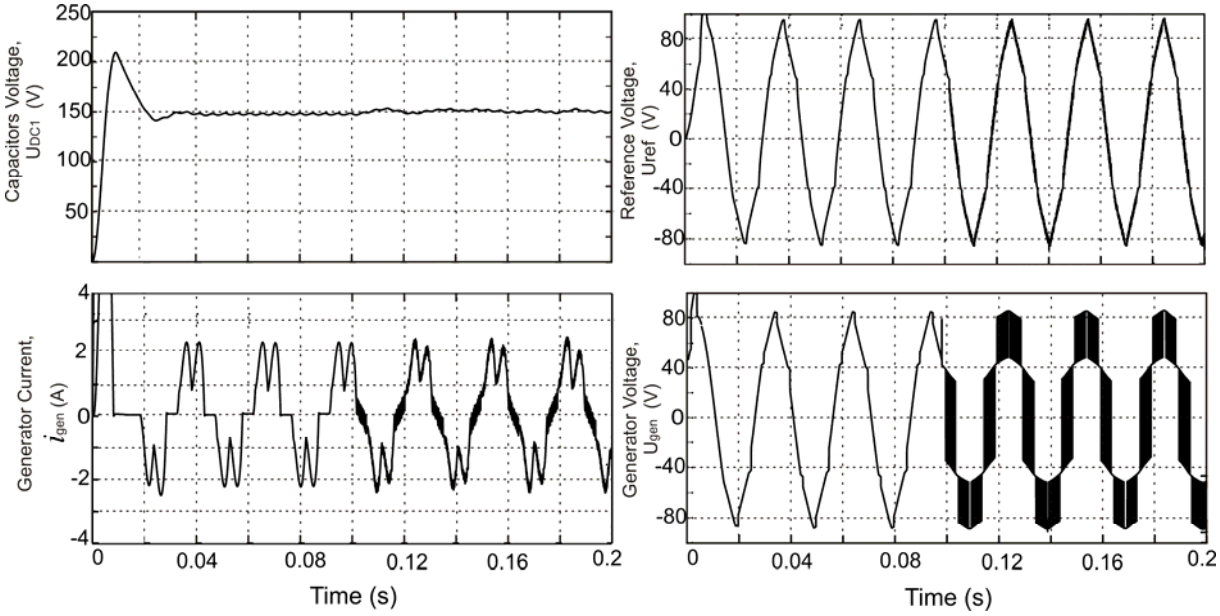


Fig. 2.9. Generator side DC link voltage U_{DC1}, PMSG current i_a, and voltage U_{gen} and filtered generator voltage U_{ref} at 330 W

The third simulation was performed at maximal speed and power of the PMSG: 510 rpm and 1250 W, respectively (Fig. 2.10). Since the nominal speed of the generator is 375 rpm, it was required to verify the generator's ability to produce the power necessary at that speed. The amplitude of the generator's output voltage U_{gen} reaches 250 V. PFC control is not used in this mode and THD of generator current is about 28%.

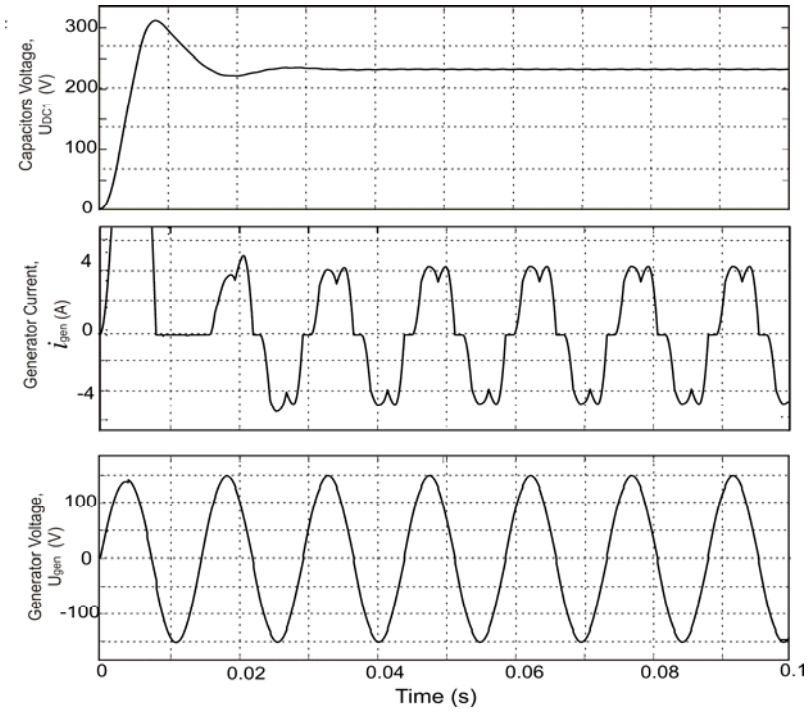


Fig. 2.10. Generator-side DC link voltage U_{DC1}, PMSG current i_a and voltage U_{gen}, at 1250 W

The test setup for generator side inverter is shown in Fig. 2.11. It consists of active rectifier, Hall sensors for current measurement and optically isolated voltage measurement system, digital control system and optically isolated drivers for IGBT transistors.

A series of experiments were performed to verify the proper operation of the PMSG with the controller. Experiments with the controlled rectifier were performed according to the simulation parameters. Control was realized by controlling six transistors with a fixed duty cycle at 20 kHz switching frequency. It should be noted, that additional serial inductance was added in order to smooth output voltage of generator. It is necessary for proper measurement of voltage that is used as reference signal in control system. Additionally the inductors ensure lower current ripple.

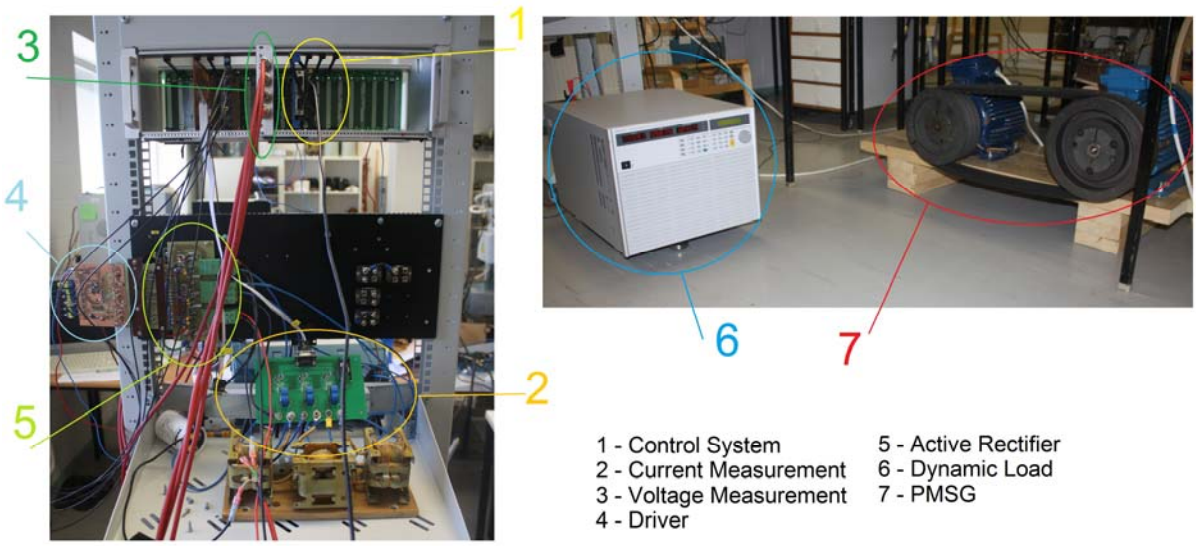


Fig. 2.11. Laboratory test setup for generator side inverter tests

The first experimental test was performed at rated speed conditions, with the generator speed at 315 rpm and turbine power at 330 W. At this point the amplitude of the generator voltage U_{gen} is 150 V and boost control are not needed (Fig. 2.12.). Opposite site of this situation is current shape that doesn't coincident with voltage shape. It is explained by not enough high DC link voltage with respect to input voltage. It proved simulation results.

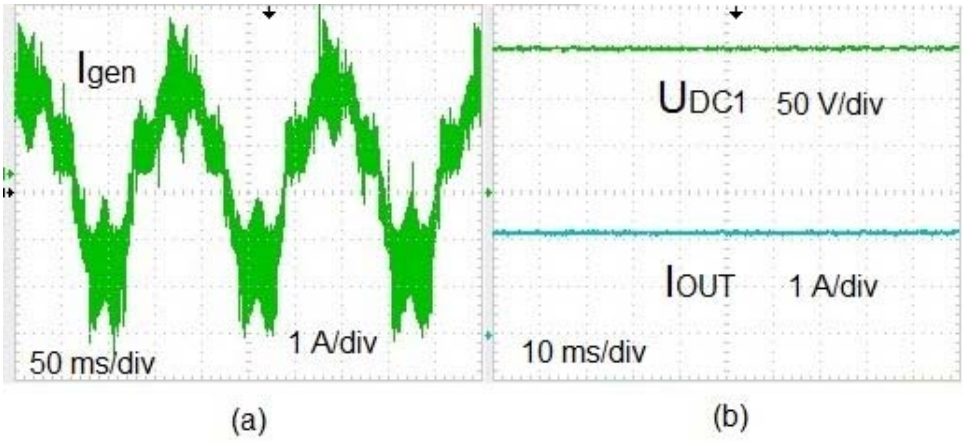


Fig. 2.12. Experimental results: PMSG current (a) and generator side DC link voltage and current (b) at 330 W

The second test was performed at maximal speed and power of the PMSG: 510 rpm and 1250 W, respectively (Fig. 2.13.). Since the nominal speed of the generator is 375 rpm, it was required to verify the generator's ability to produce the power necessary at that speed. The amplitude of the generator's output voltage reaches 250 V. PFC control is not possible in this mode.

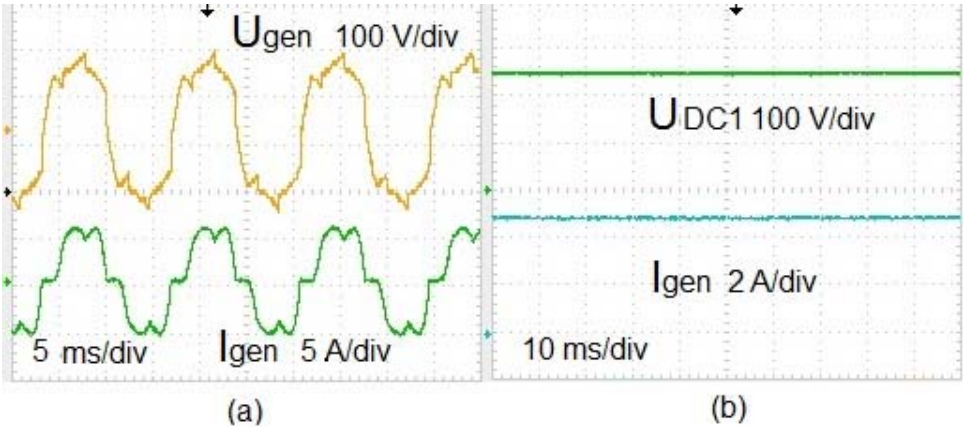


Fig. 2.13. Experimental results: PMSG voltage and current (a) and generator-side DC link voltage and current (b) at 1250 W

From experimental results is concluded that the controlled rectifier operates in close to expected mode. Limitations connected with voltage distortion during transistor switching can be eliminating by improvement of signal filtering. The distortions of measured voltage have influence on the control algorithm performance since measurement voltage is used as reference signal. Some passive filter can be used top improve the measured signals and overall performance of control system.

2.2. qZS based DC/DC converter with HF isolation

The qZSI is derived from a traditional Z-source inverter (ZSI) [45] and has two distinctive advantages as compared to ZSI, such as continuous DC current drawn from the source and lower operating voltage of the capacitor C_2 [2]. Practically, qZSI is a traditional PWM inverter coupled with a special quasi-Z-source network (qZS-network). As seen from Fig. 2.14., the qZS-network consists of two capacitors C_1 and C_2, two inductors L_1 and L_2 and a diode D_1. The operation principle of the qZSI will be analyzed in detail in the next sections.

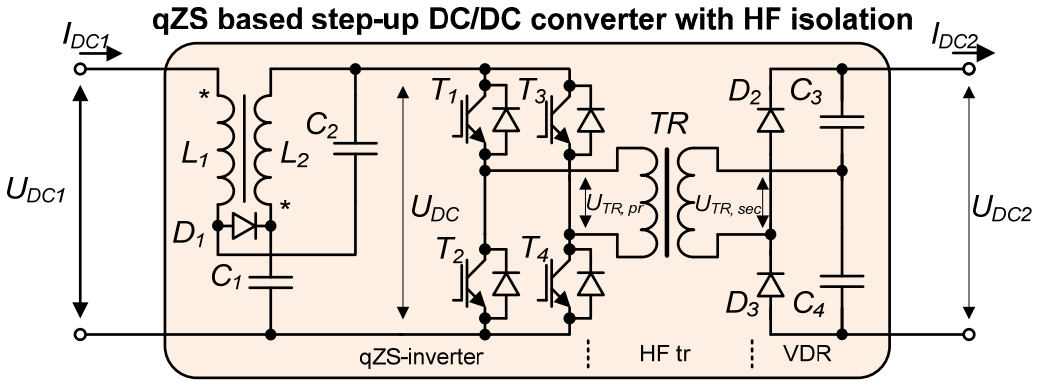


Fig. 2.14. qZS based step-up DC/DC converter with HF isolation

The high-frequency step-up isolation transformer provides the required galvanic isolation of the input and output sides of the converter. Transformer's primary winding is connected to the output terminals of qZSI, while the secondary side is connected to the voltage doubler rectifier (VDR). The VDR is derived from the full- bridge rectifier (B4U) by the replacement of diodes in one leg by the capacitors (C_3 and C_4) with equal capacity [72]. The resulting advantages of the VDR over the traditional B4U scheme are the doubling effect of the secondary winding voltage of the isolation transformer and reduced power dissipation due to smaller number of rectifying diodes and full elimination of the smoothing inductor. Moreover, the dynamic performance and stability of VDR could be increased.

2.2.1. Operating modes qZS based DC/DC converter

The main function of the HF isolation converter is to stabilize the grid side inverter voltage U_{DC2} despite the variations of the first DC link voltage U_{DC1}. By keeping the DC-link voltage constant the PWM inverter could be operated with a fixed duty cycle value, thus ensuring constant volt-second and flux swing of the isolation transformer.

In accordance with the input voltage (generator side DC link voltage) the operating modes of the proposed DC/DC converter could be broadly categorized as *non-shoot-through* and *shoot-through* operating modes (Fig. 2.15).

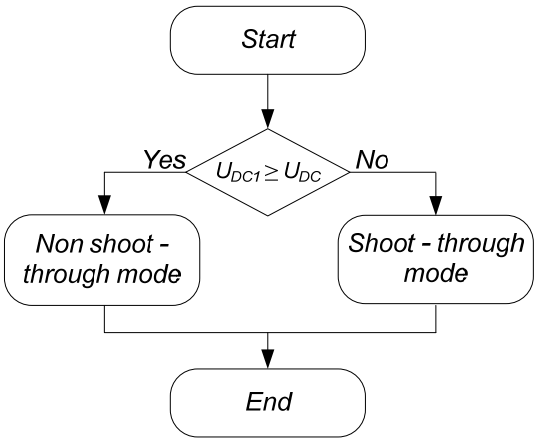


Fig. 2.15. Flow chart of operating modes of qZSI based DC/DC converter

Non-shoot-through operating mode

If the voltage is equal or higher than the desired DC-link voltage, the converter starts to operate in the non-shoot-through mode. In this mode the qZSI operates as a traditional VSI performing only the buck function of the input voltage. The operating period of the qZSI in the non-shoot-through mode consists of the combination of active and zero states. During active (energy transfer) states the power switches of the inverter bridge are gated alternately in pairs (T_1, T_4 and T_2, T_3) and power is transferred from the DC-link to the isolation transformer (Fig. 2.16.). During zero states the primary winding of the isolation transformer is shorted either through the upper switches (T_1, T_3) or the bottom switches (T_2, T_4) of the inverter bridge (Fig. 2.17) and the transformer sees no voltage from the inverter.

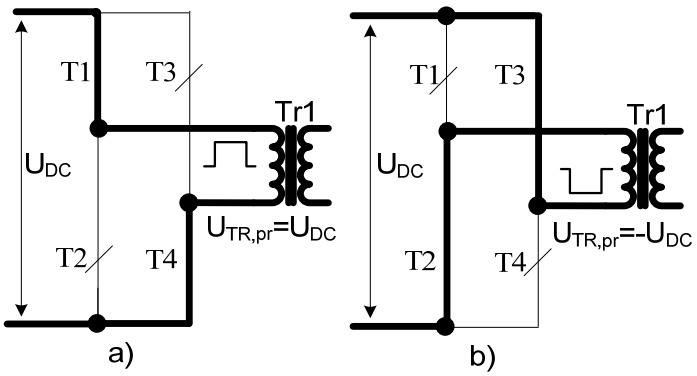


Fig. 2.16. Equivalent circuit during active states: positive (a) and negative (b) half-cycles

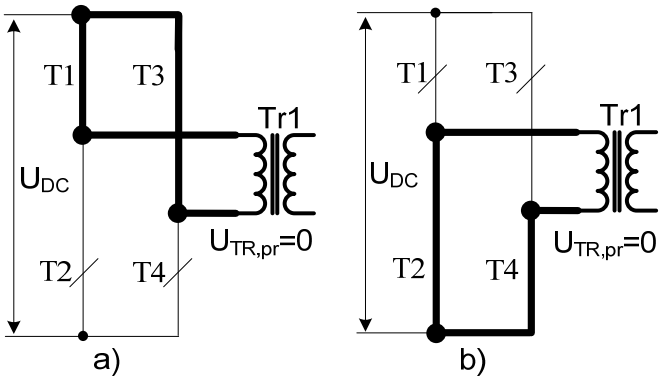


Fig. 2.17. Equivalent circuit during zero-states created by upper (a) and lower (b) switches

The switching state diagram of the proposed converter during the non-shoot-through mode is presented in Fig. 2.18. It is seen that in the discussed algorithm zero states are created by the upper switches of the inverter bridge (T_1 and T_3). The HF inverter switching states sequence presented in Table 2.2 shows that the upper and lower switches operate with same switching frequency.

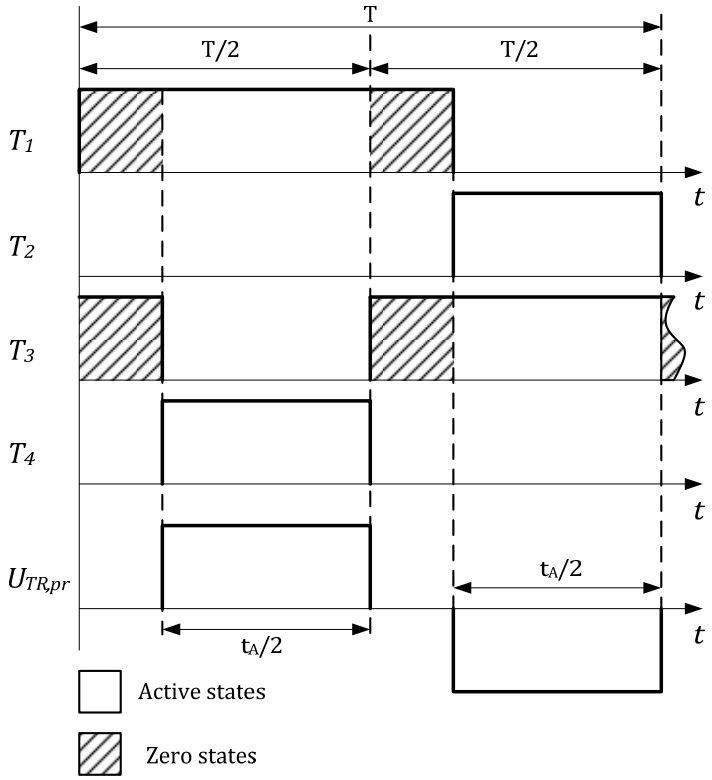


Fig. 2.18. Operation principle of the qZSI in the non-shoot-through mode

Table 2.2

PWM switching states sequence of the qZSI during the non-shoot-through operating mode

State	T1	T2	T3	T4
zero state	1	0	1	0
active state 1	1	0	0	1
zero state	1	0	1	0
active state 2	0	1	1	0

The operating period of the PWM inverter during the non-shoot-through mode consists of an active state t_A and a zero state t_Z:

$$T = t_A + t_Z \tag{12}$$

Equation (12) could also be represented as

$$\frac{t_A}{T} + \frac{t_Z}{T} = D_A + D_Z = 1, \tag{13}$$

where D_A - is the duty cycles of an active state

D_Z - is the duty cycle of an zero state.

Shoot-through operating mode

If the generator side DC link voltage drops below the predefined DC link voltage level U_{DC} the converter begins to operate in the shoot-through mode. The varying voltage of the generator side DC link is preregulated to a desired DC-link voltage level by adjusting the shoot-through duty cycle. Afterwards the isolation transformer is being supplied from the inverter with a voltage of constant amplitude, as described in the previous section.

To boost the input voltage during the shoot-through operating mode the special switching state – shoot-through state - is implemented in the HF inverter control. During the shoot-through states the primary winding of the isolation transformer is shorted through both the upper and lower switches of any one phase leg (i.e., both devices are gated on) or both phase legs (Fig. 2.19). This shoot-through state (or vector) is forbidden in the traditional VSIs, because it would cause a short circuit of DC capacitors and destruction of power switches. The unique two-port network – the qZS-network (see Fig. 2.14) – makes the shoot-through states possible, effectively protecting the circuit from damage. Moreover, the shoot-through states are used to boost the magnetic energy stored in the DC side inductors L_1 and L_2 without short-circuiting the DC capacitors C_1 and C_2. This increase in the inductive energy in turn provides the boost of voltage seen on the inverter output during the active states of the inverter.

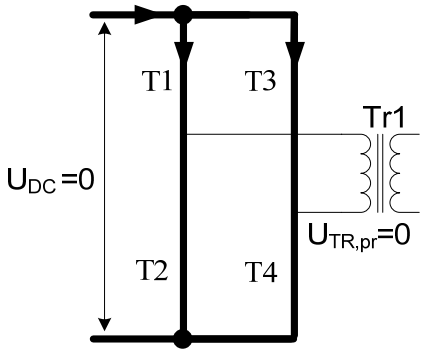


Fig. 2.19. Inverter equivalent scheme during the shoot-through state

The switching state diagram of the proposed converter during the shoot-through mode is presented in Fig. 2.20. To control the shoot-through states two reference signals (U_p and U_n) were introduced. If the triangle waveform is greater than U_p or lower than U_n, the inverter switches turn into the shoot-through state. Thus, in the proposed shoot-through PWM control method, to reduce the current stress of the switches, the shoot-through states are created by simultaneous turning on of all inverter switches (Fig. 2.19). The shoot-through time is evenly split into two intervals of half the duration. During the shoot-through states the voltage across inverter bridge drops to zero.

The PWM switching states sequence presented in Table 2.3 shows that the upper and lower switches operate with different switching frequencies. The switching frequency of the upper switches (T_1 and T_3) in the shoot-through mode is equal to the fundamental frequency of the isolation transformer, while the switching frequency of the lower switches (T_2 and T_4) is three times higher than that of T_1 and T_3

Table 2.3

PWM switching states sequence of the qZSI during the shoot-through operating mode

State	T1	T2	T3	T4
zero state	1	0	1	0
shoot-through	1	1	1	1
zero state	1	0	1	0
active state 1	1	0	0	1
zero state	1	0	1	0
shoot-through	1	1	1	1
zero state	1	0	1	0
active state 2	0	1	1	0

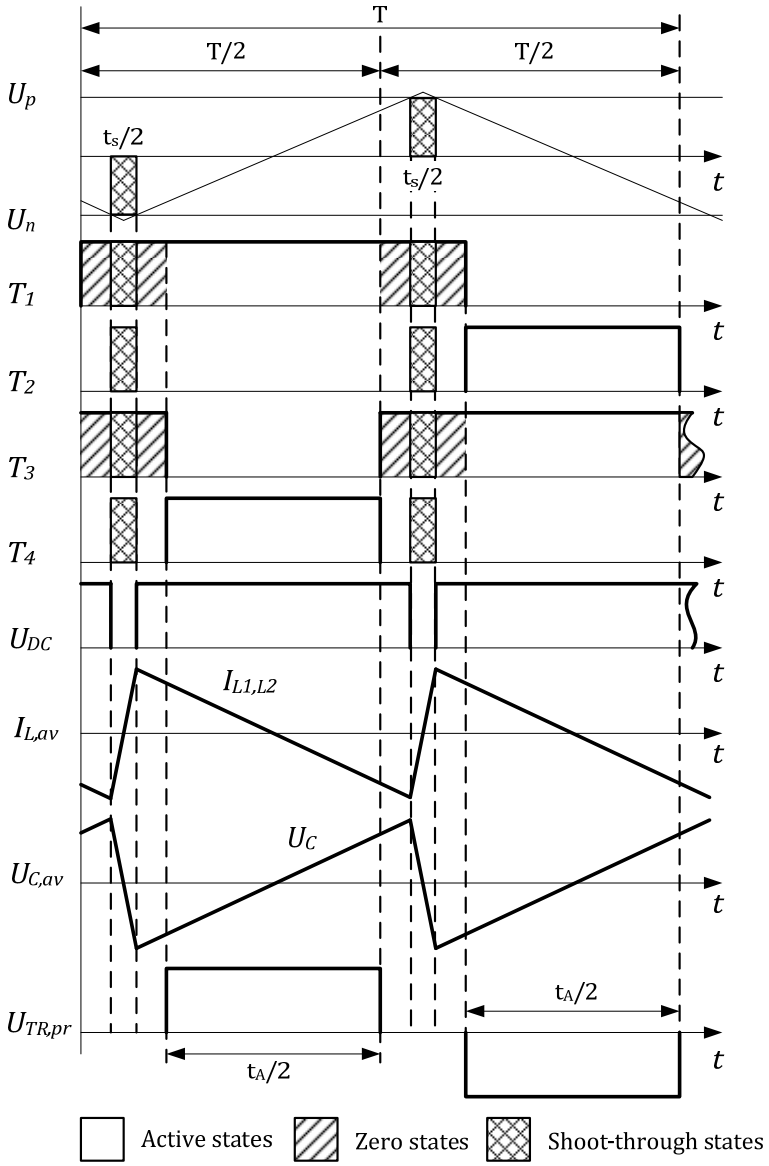


Fig. 2.20. Operation principle of the qZSI in the shoot-through mode

The operating period of the PWM inverter during the shoot-through mode consists of an active state t_A, a zero state t_Z and a shoot-through state t_S:

$$T = t_A + t_Z + t_S \tag{14}$$

Equation (14) could also be represented as

$$\frac{t_A}{T} + \frac{t_Z}{T} + \frac{t_S}{T} = D_A + D_Z + D_S = 1, \tag{15}$$

where D_A - duty cycle of the active state;

D_Z - duty cycle of the zero state;

D_S - duty cycles of the shoot-through state.

Operation of voltage-doubler rectifier

To reduce the turns ratio of the isolation transformer the voltage doubler rectifier (VDR) was implemented on the secondary side of the converter. In contrast to the traditional full-bridge rectifier, two diodes of one leg in the VDR topology are replaced by the capacitors. The operation principle of the VDR is explained in Fig. 2.21. and Fig. 2.22.

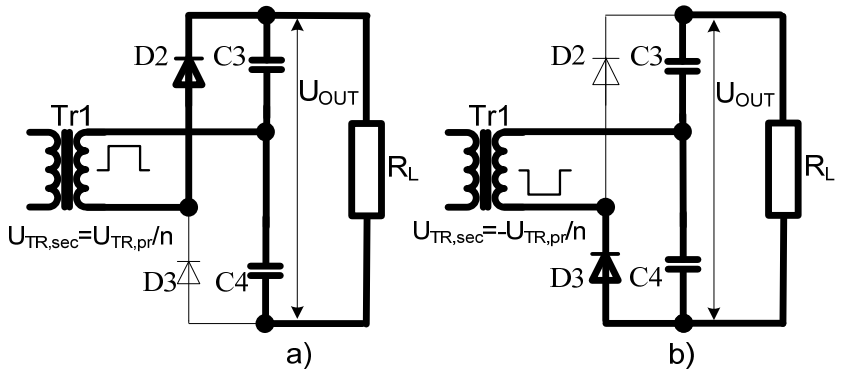


Fig. 2.21. Operation principle of VDR

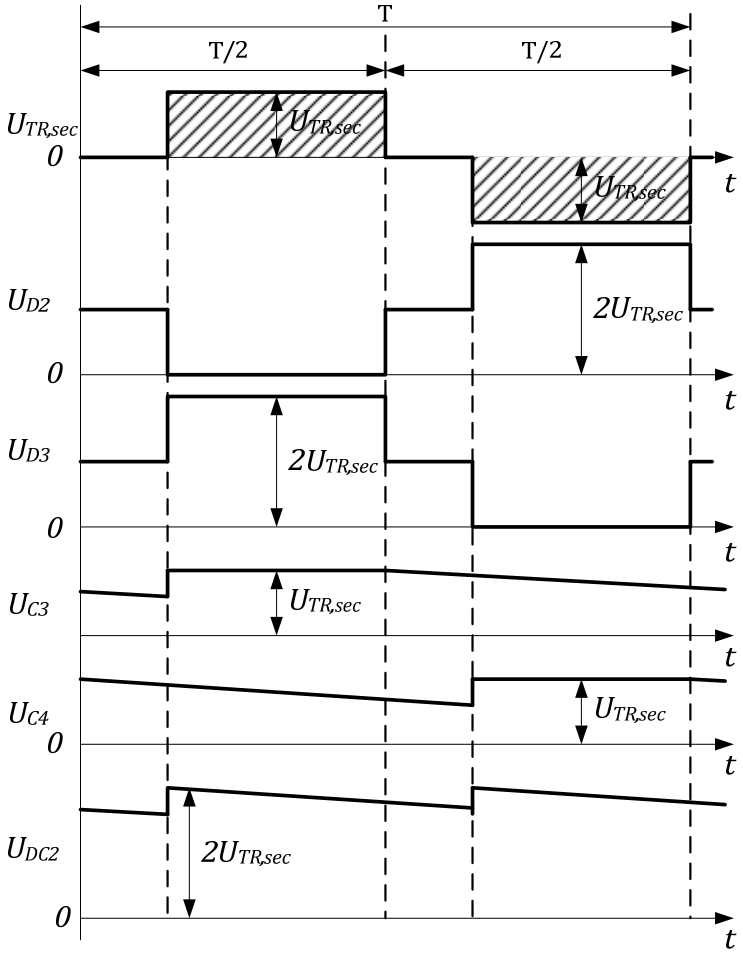


Fig. 2.22. General waveforms of VDR

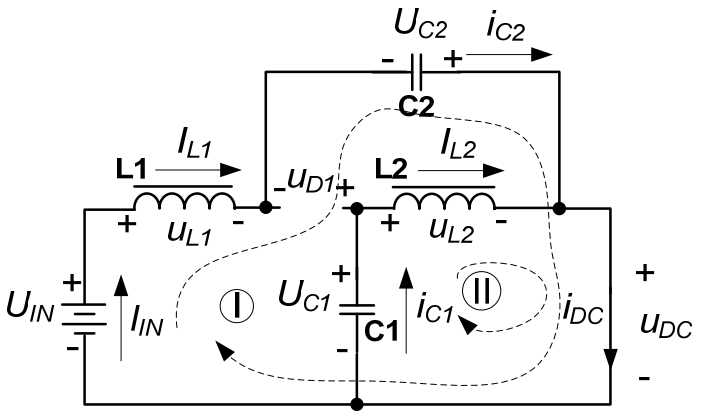
During the positive half cycle, the capacitor C_3 is charged through the diode D_2 to the peak secondary voltage of the isolation transformer (Fig. 2.21*a*). During the negative half cycle the capacitor C_4 is charged through diode D_3 (Fig. 2.21*b*). At every time instant the output voltage (U_{DC2}) from this circuit will be the sum of the two capacitor voltages (Fig. 2.22.), or twice the peak voltage ($U_{TR,sec}$) of the secondary winding of the isolation transformer:

$$U_{DC2} = 2 \cdot U_{TR,\text{sec}} \,. \tag{16}$$

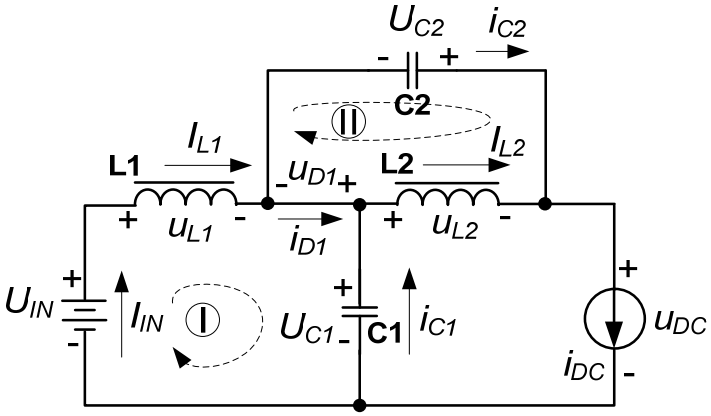
Operating principle of the qZSI during the shoot-through mode

As shown in Fig. 2.14., the voltage-fed qZSI with continuous input current is built in the converter input side and it has a unique property: it can boost the input voltage utilizing a special switching state – the shoot-through state (Fig. 2.17.). The shoot-through state is a time interval when both switches of both inverter legs are conducting.

In the shoot-through operation mode there are two general power conversion states: shoot-through (voltage boost in primary side) and active (power transfer to secondary side) state.



(a)



(b)

Fig. 2.23. Equivalent circuits of the qZSI during the shoot-through (a) and active (b) states

The equivalent schemes of the qZSI during the shoot-through and active state are presented in Fig. 2.23.[73]. All the polarities, voltages and currents are defined with arrows and polarity signs.

From Fig. 2.23.*a*, which represents the shoot-through state of the qZSI with duration t_S, we can obtain

$$u_{L1} = U_{C2} + U_{IN}, \quad u_{L2} = U_{C1}, \tag{17}$$

$$u_{DC} = 0, \quad u_{D1} = U_{C1} + U_{C2}. \tag{18}$$

From Fig. 2.23.*b*, which represents the active state of the qZSI with the duration of (T-t_S), we can obtain

$$u_{L1} = U_{IN} - U_{C1}, \quad u_{L2} = -U_{C2}, \tag{19}$$

$$u_{DC} = U_{C1} - u_{L2} = U_{C1} + U_{C2}, \quad u_{D1} = 0. \tag{20}$$

At the steady state the average voltage of the inductor over one switching period is zero. Thus, from equations (17) and (19) we can obtain

$$\begin{cases} U_{L1} = u_{L1} = \dfrac{t_S \cdot (U_{C2} + U_{IN}) + (T - t_S) \cdot (U_{IN} - U_{C1})}{T} = 0 \\ U_{L2} = u_{L2} = \dfrac{t_S \cdot (U_{C1}) + (T - t_S) \cdot (-U_{C2})}{T} = 0 \end{cases}. \tag{21}$$

Accordingly,

$$U_{C1} = \frac{1 - \frac{t_S}{T}}{1 - 2 \cdot \frac{t_S}{T}} \cdot U_{IN} \text{ and } U_{C2} = \frac{\frac{t_S}{T}}{1 - 2 \cdot \frac{t_S}{T}} \cdot U_{IN}. \tag{22}$$

The peak DC-link voltage across the inverter bridge is

$$\hat{u}_{DC} = U_{C1} + U_{C2} = \frac{1}{1 - 2 \cdot \frac{t_S}{T}} \cdot U_{IN} = B \cdot U_{IN}, \tag{23}$$

where B - is the boost factor of the qZSI:

$$B = \frac{1}{1 - 2 \cdot \frac{t_S}{T}}. \tag{24}$$

Using the system power rating P we can obtain the average current of inductors L_1 and L_2:

$$I_{L1,av} = I_{L2,av} = I_{IN,av} = \frac{P}{U_{IN}}, \tag{25}$$

where U_{IN} - is the input voltage of the converter.

To obtain the necessary currents of the qZSI we can use Kirchhoff`s current law and equation (23):

$$I_{C1,av} = I_{C2,av} = I_{DC,av} - I_{L1,av}; \tag{26}$$

$$I_{D1,av} = 2I_{L1,av} - I_{DC,av}. \tag{27}$$

The operating voltages and average currents of the qZSI during active and shoot-through states are shown in Table 2.4. For the better appearance the shoot-through time interval t_S was replaced with the shoot-through duty cycle $D_S=t_S/T$.

Table 2.4

Operating voltages and average currents of the qZSI

State	Active	Shoot-through
Inductor voltage ($u_{L1}=u_{L2}$)	$-\frac{D_S}{1-2\cdot D_S}\cdot U_{IN}$	$\frac{1-D_S}{1-2\cdot D_S}\cdot U_{IN}$
DC-link voltage (u_{DC})	$\frac{1}{1-2\cdot D_S}\cdot U_{IN}$	0
DC-link current ($I_{DC,av}$)	$\frac{P\cdot(1-2\cdot D_S)}{U_{IN}}$	$\frac{2\cdot P}{U_{IN}}\cdot D_S$
Diode D1 voltage (u_{D1})	0	$\frac{1}{1-2\cdot D_S}\cdot U_{IN}$
Capacitor C1 voltage (U_{C1})	$\frac{1-D_S}{1-2\cdot D_S}\cdot U_{IN}$	
Capacitor C2 voltage (U_{C2})	$\frac{D_S}{1-2\cdot D_S}\cdot U_{IN}$	
Input current ($I_{IN,av}$)	$\frac{P}{U_{IN}}$	
Inductor current ($I_{L1,av}=I_{L2,av}$)	$\frac{P}{U_{IN}}$	
Capacitor current ($I_{C1,av}=I_{C2,av}$)	$I_{DC,av}$ - $I_{L1,av}$	
Diode current ($I_{D1,av}$)	$2\cdot I_{L1,av}$ - $I_{DC,av}$	

Design issues of the qZS network

The qZS-network consists of two inductors, two capacitors and one diode, which should be properly dimensioned to ensure the correct operation of the network during shoot-through states. As seen from Fig. 2.20., the shoot-through time is evenly split into two intervals of half the duration and the operating frequency of the qZS-network is twice the fundamental frequency of the isolation transformer.

Dimensioning of capacitors

The main purpose of capacitors C_1 and C_2 is to absorb the current ripple and limit the voltage ripple across the inverter bridge. The voltage ripple across the capacitor can be roughly calculated by

$$\Delta U_C = \frac{I_{L,av} \cdot \Delta t}{C}, \tag{28}$$

where $I_{L,av}$ - average current through the inductor;

C - capacitance of qZS capacitors;

Δt - the time interval of the shoot-through state.

In the proposed shoot-through PWM control method the shoot-through time is evenly split into two intervals of half the duration. During active states both capacitors of the qZS-network are in series (Fig. 2.23.*b*). Assuming that the capacitance should be the same for each capacitor, the capacitance needed to limit the peak to peak DC-link voltage ripple by $r_{V,DC}$ could be calculated as

$$C = \frac{2 \cdot P \cdot D_S}{U_{IN} \cdot U_C \cdot f \cdot r_{V,DC}}, \tag{29}$$

where P - power rating of the converter;

U_{IN} - input voltage;

U_C - capacitor's voltage;

D_S - duty cycle of shoot-through states;

f - operation frequency of the qZSI;

$r_{V,DC}$ - desired peak to peak voltage ripple across the DC-link ($U_{p\text{-}p}/U_{av}$).

Dimensioning of inductors

The inductor in the qZSI network will limit the current ripple through the switches during the shoot-through states. Choosing an acceptable peak to peak current ripple r_C the inductance can be calculated by

$$L = \frac{U_{C1} \cdot D_S \cdot U_{IN}}{P \cdot f \cdot r_C}, \tag{30}$$

where U_{C1} - is the capacitor's C1 voltage;

D_S - is the duty cycle of shoot-through states;

f - is the operation frequency of the qZSI;

r_C - is the desired peak to peak current ripple through the inductor ($I_{p\text{-}p}/I_{av}$).

To minimize the size and weight of the inductors, the two inductors could be built together on one core, thus forming the coupled inductor [15] (Fig. 2.24). For a single coil on one core, the flux through core is

$$\varphi = E \cdot N \cdot i_L, \tag{31}$$

where E - is a constant related to the core material and dimensions;

N - is the number of turns of the coil;

i_L - is the current through the coil.

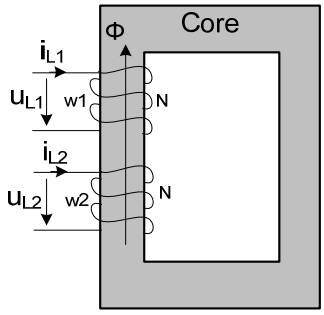


Fig. 2.24. Coupled inductor

The inductance of the coil is

$$L = \frac{N \cdot \phi}{i_L} = E \cdot N^2, \tag{32}$$

In the voltage-fed qZSI the currents through inductors L_1 and L_2 are always exactly the same in terms of waveform and magnitude. For two coils on one core with exactly the same current, i, the flux through the core is

$$\phi = 2 \cdot E \cdot N \cdot i_L \,. \tag{33}$$

The resulting inductance of each winding when supplying exactly the same current to the two windings is

$$L = \frac{N \cdot \phi}{i_L} = 2 \cdot E \cdot N^2 \,. \tag{34}$$

It is seen from Eq. (33) that the inductance of each winding is doubled. Therefore, for the same operating conditions we need to build two windings with twice smaller inductance than in the case of separate inductors.

Dimensioning of diode

The diode D_1 should be chosen taking into account the maximal voltage $u_{D1,max}$ and average current $I_{D1,av}$ through it. During the shoot-through states the diode D_1 is reverse-biased (Fig. 2.23.*a*) and neglecting transients the maximal blocking voltage is

$$u_{D1,\max} = B \cdot U_{IN} = U_{IN} \cdot \frac{1}{1 - 2 \cdot D_S} \,. \tag{35}$$

Average diode current could be found from Table 3:

$$I_{D1,av} = 2 \cdot I_{L1,av} - I_{DC,av} = \frac{2 \cdot P}{U_{IN}} - \frac{P}{U_{IN}} = \frac{P}{U_{IN}} \,, \tag{36}$$

where P - is the power rating of the converter;

U_{IN} - is the input voltage;

U_{DC} - is the DC-link voltage;

D_S - is the shoot-through duty cycle.

Maximal diode current could be found as

$$I_{D1,\max} = I_{L1,\max} + I_{L2,\max} = I_{DC,\max} \,. \tag{37}$$

During the diode selection special attention should be paid to the switching properties of it, i.e. the fast recovery diodes should be preferred to ensure proper recovery times. The forward voltage drop U_{FVD} is another important issue, because the high values of U_{FVD} could cause high conduction losses during active states, which, in turn, could seriously affect the efficiency of the converter.

HF inverter

In the PWM inverter, each switching device has to be selected according to the maximum voltage applied and the peak and average current going through it. The maximal voltage (neglecting transients) that should be taken as a basis for choosing power switches should be found as a multiplication of the input voltage U_{IN} and the boost factor B:

$$u_{DC,\max} = B \cdot U_{IN} = U_{IN} \cdot \frac{1}{1-2 \cdot D_S}. \tag{38}$$

The current through the inverter switches consists of two elements, the current to the isolation transformer during active states $I_{A,av}$ and the current through them when the circuit is in the shoot-through state $I_{S,av}$ (Fig. 2.25):

$$I_{SW,av} = I_{A,av} + I_{S,av}. \tag{39}$$

The current during shoot-through states in terms of average is evenly distributed between both inverter arms, as shown in Fig. 2.19. The average current value in the shoot-through period through each switch is

$$I_{S,av} = \frac{2 \cdot I_{L,av}}{2} \cdot \frac{D_S}{2} = \frac{P \cdot D_S}{U_{IN}}, \tag{40}$$

where $I_{L,av}$ - is the average current through the inductors;

D_S - is the shoot-through duty cycle;

U_{IN} - the input voltage of the converter;

P - the power rating of the converter.

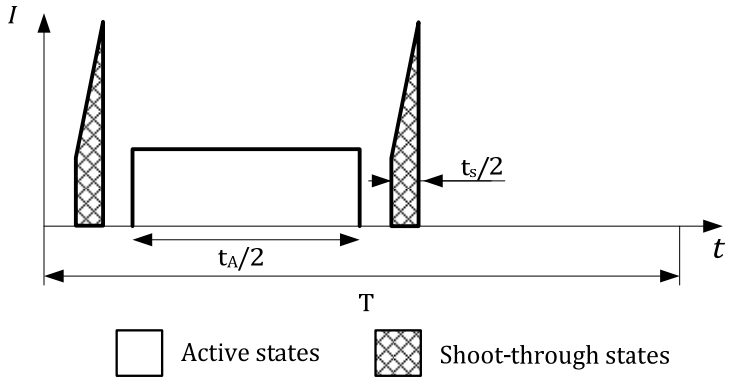


Fig. 2.25. Operating current waveform of the inverter switch during one switching period

While in active states the average current is the same as in a conventional PWM inverter:

$$I_{A,av} = \frac{I_{DC,av}}{2} = \frac{P}{2 \cdot U_{DC}}, \tag{41}$$

where $I_{DC,av}$ - is the average DC-link current;

U_{DC} - is the DC-link voltage;

P - is the power rating of the converter.

The overall average current through inverter switches is

$$I_{SW,av} = \frac{P \cdot D_S}{U_{IN}} + \frac{P}{2 \cdot U_{DC}} = \frac{P}{2 \cdot U_{IN}}. \tag{42}$$

The peak current through the switches occurs during shoot-through states:

$$I_{SW,\max} = I_{L,av} \cdot \left(1 + \frac{r_C}{2}\right) = \frac{P}{U_{IN}} \cdot \left(1 + \frac{r_C}{2}\right), \tag{43}$$

where $I_{L,av}$ - is the average current through the inductors;

r_C - is the peak to peak current ripple through the inductors during maximum power operation ($I_{p\text{-}p}/I_{av}$).

Isolation transformer

The turns ratio n of an isolation transformer is defined as a relation of primary and secondary winding voltages:

$$n = \frac{U_{TR,pr}}{U_{TR,\text{sec}}} = \frac{U_{DC}}{U_{OUT}/2}, \tag{44}$$

where $U_{TR,pr}$ - is the primary winding voltage;

$U_{TR,sec}$ - is the secondary winding voltage;

U_{DC} - is the DC-link voltage;

U_{OUT} - is the average output voltage of the converter.

Replacing the U_{DC} value by that from Table 2.1 we can obtain:

$$n = \frac{U_{IN} \cdot B \cdot 2}{U_{OUT}} = \frac{2 \cdot U_{IN}}{(1 - 2 \cdot D_S) \cdot U_{OUT}}, \tag{45}$$

where D_S - is the shoot-through duty-cycle;

U_{IN} - is the input voltage of the converter.

Taking into consideration Equation (45), we can express the output voltage of the proposed converter for every operating point within the shoot-through operating mode:

$$U_{OUT} = \frac{2 \cdot U_{IN}}{(1 - 2 \cdot D_S) \cdot n}. \tag{46}$$

Voltage doubler rectifier

To provide correct operation of the VDR and ensure the voltage doubling effect the capacitors C_3 and C_4 (Fig. 2.14.) should be properly dimensioned. To limit the peak to peak voltage ripple on these capacitors by $r_{V,OUT}$, the capacitance should be

$$C = \frac{P \cdot \left(1 - \frac{D_A}{2}\right)}{(U_{OUT})^2 \cdot f \cdot r_{V,OUT}}, \tag{47}$$

where P - is the power rating of the converter;

U_{OUT} - is the output voltage;

D_A - is the duty cycle of active state;

f - is the operation frequency of the Qzsi;

$r_{V,OUT}$ - is the peak to peak voltage ripple in the output of the VDR ($U_{p\text{-}p}/U_{OUT}$).

When reverse-biased, the diodes D_2 and D_3 should block voltage twice the amplitude voltage of the secondary winding of the isolation transformer (neglecting transients):

$$u_{D2,\max} = u_{D3,\max} = 2 \cdot U_{TR,\sec} = U_{OUT}. \tag{48}$$

The peak current of the diodes is typically limited by the system parameters such as transformer leakage inductance, equivalent series resistance (ESR) of capacitors, active resistance of wires, etc. and cannot be directly calculated. However, the average current of diodes is equal to the output average current and could be found as:

$$I_{D2,av} = I_{D3,av} = \frac{P}{U_{OUT}}. \tag{49}$$

As in the case of input diode D_1, for ensuring higher efficiency of the converter the diodes for the VDR should be selected with special attention to the recovery times and forward voltage drop values.

2.2.2. Discontinuous conduction mode of qZS inverter.

As it is seen from Fig. 2.1., the proposed qZS-inverter has the input inductor L_1 that buffers the source current. It means that in the continuous conduction mode (CCM) the input current never drops to zero during the shoot-through states. However, in the case of small loads, relatively low switching frequency and low inductance values of L_1 and L_2, the qZS-inverter could start to operate in the discontinuous conduction mode (DCM) and the input current falls to zero during some part of the switching period. In the current application, similar conditions could appear during the operation of a wind turbine near the cut-in region, when the PMSG power drops to minimum [8].

The operating period of the qZS-inverter in the DCM generally consists of an active state t_A, a shoot-through state t_S and a discontinuous conduction state t_D

$$\frac{t_A}{T}+\frac{t_S}{T}+\frac{t_D}{T}=D_A+D_S+D_D=1, \tag{50}$$

where D_A - duty cycles of active;

D_S - shoot-through state;

D_D - discontinuous conduction state.

The equivalent circuit of the discontinuous conduction state is similar to the active states (Fig. 2.16.*b*), the only difference is that the diode D_1 stops conducting at that time interval. The equivalent circuits of the qZS-inverter in the shoot-through and active states remain the same as in Fig. 2.17

When the converter is in a discontinuous conduction state t_D, the voltages of the inductors L_1 and L_2 are equal to zero. For the DCM, Eq. (21) could be extended as follows:

$$\begin{cases} U_{L1}=\overline{u}_{L1}=D_S\cdot(U_{C3}+U_{DC1})+D_A\cdot(U_{DC1}-U_{C2})+D_D\cdot 0=0 \\ U_{L2}=\overline{u}_{L2}=D_S\cdot(U_{C2})+D_A\cdot(-U_{C3})+D_D\cdot 0=0 \end{cases}, \tag{51}$$

where D_A - duty cycles of active;

D_S - shoot-through state;

D_D - discontinuous conduction state.

In contrast to the CCM the operating voltage of the capacitor C_2 during the DCM will increase:

$$U_{C2}=\frac{1-D_S-D_D}{1-2\cdot D_S-D_D}\cdot U_{DC1}. \tag{52}$$

That, in turn, will lead to an increased peak value of the DC link voltage during the DCM, causing the "overboost effect" of the input voltage:

$$\hat{U}_{DC(DCM)} = U_{C2} + U_{C3} = \frac{1 - D_D}{1 - 2 \cdot D_S - D_D} \cdot U_{DC1}. \quad (53)$$

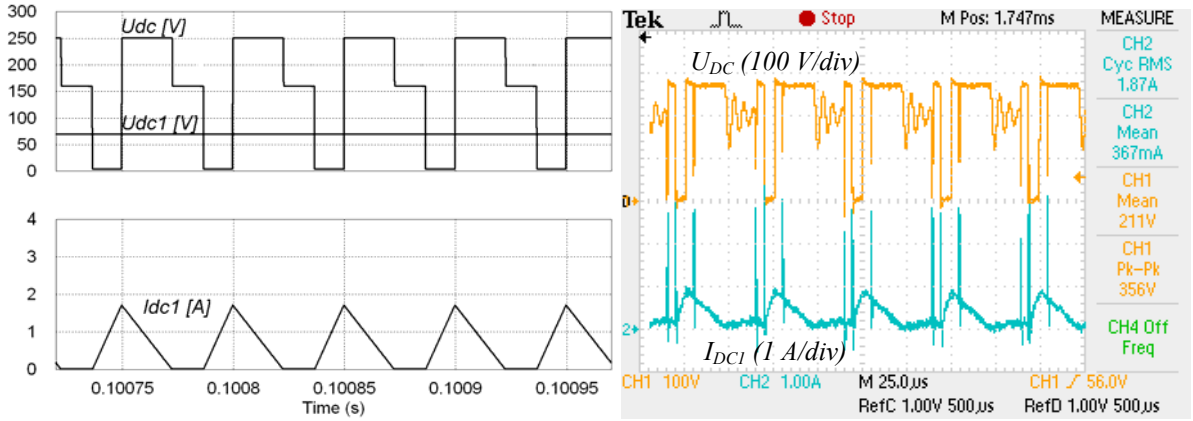
The appearance of the DCM in the experimental setup is demonstrated in Fig.2.26. The generator side DC link voltage was set to 150 V that corresponds to the cut-in and rated wind speed conditions. The load that corresponds to the turbine power at cut-in is 40 W. In order to compensate the increase of the DC link voltage caused by the DCM the shoot-through duty cycle D_S was reduced from the demanded 0.2 to 0.12. It is seen from Fig. 2.26 that the peak DC link voltage U_{DC} as well as the peak value of the primary winding voltage of the isolation transformer are 270 V that corresponds to theoretical assumptions described by (53). The input current of the converter drops to zero during the discontinuous conduction state t_D (Fig. 2.26.*a*), as predicted in the analysis. Due to long current paths in the laboratory prototype of the qZS based DC/DC converter that leads to parasitic inductances, voltage oscillations can be observed at zero input current intervals.

2.2.3. Simulation and experimental results.

In the first test the generator-side DC link voltage was set to 150 V that corresponds to the cut-in and rated wind speed conditions. The load that corresponds to the turbine power at cut-in is 40 W. The qZS based DC/DC converter operates in the discontinuous conduction mode (DCM) at such load. Since the voltage boost of the qZS based DC/DC converter is higher at the DCM than at the CCM, the shoot-through duty cycle D_S was set at 0.12 for this mode. Peak DC link voltage U_{DC} is 270 V (Fig. 2.27.) that corresponds to theoretical assumptions stated in [8]. The DCM for low power operation was chosen to reduce the size of the inductors. Transformer voltages (Fig. 2.27) repeat the shape of the intermediate DC link voltage. Due to long current paths in the laboratory prototype of the qZS based DC/DC converter that leads to parasitic inductances, the voltage oscillations can be observed at zero input current intervals.

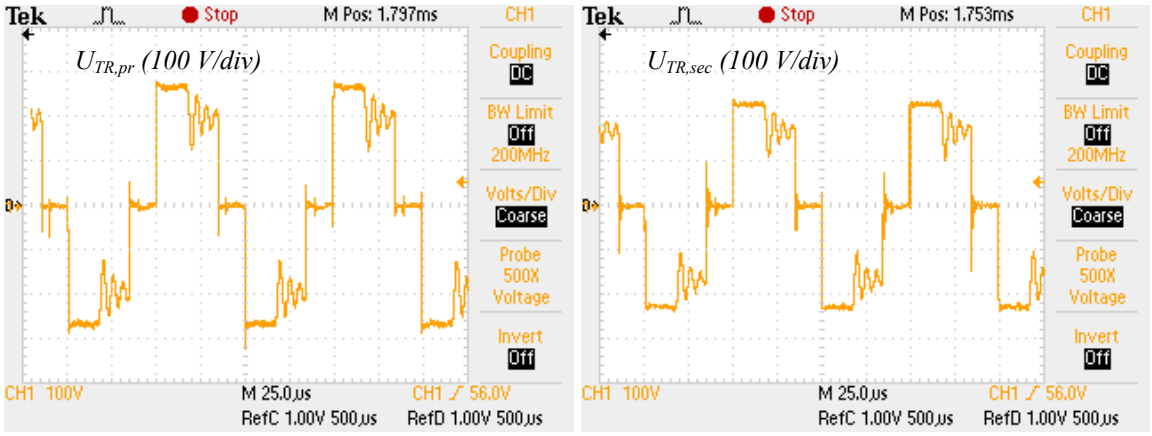
The second test was performed at the same generator-side DC link voltage (U_{DC1} = 150 V), but power was raised to 330 W that corresponds to turbine power at the rated wind speed. To boost the input voltage to the desired voltage level of the intermediate DC-link (250 V) the shoot-through duty cycle D_S was set to 0.2. Fig. 2.28. shows that the qZSI operates in the CCM, thus ensuring the demanded gain of the input voltage (U_{DC} = 250 V, as

expected). Moreover, the voltage doubler rectifier provides the demanded voltage doubling effect of the peak voltage of the secondary winding of the isolation transformer, thus ensuring the voltage of 405 V DC at the grid side DC-link (Fig. 2.28). Transformer voltages (Fig. 2.29) have not any disturbances that verify correct component selection.



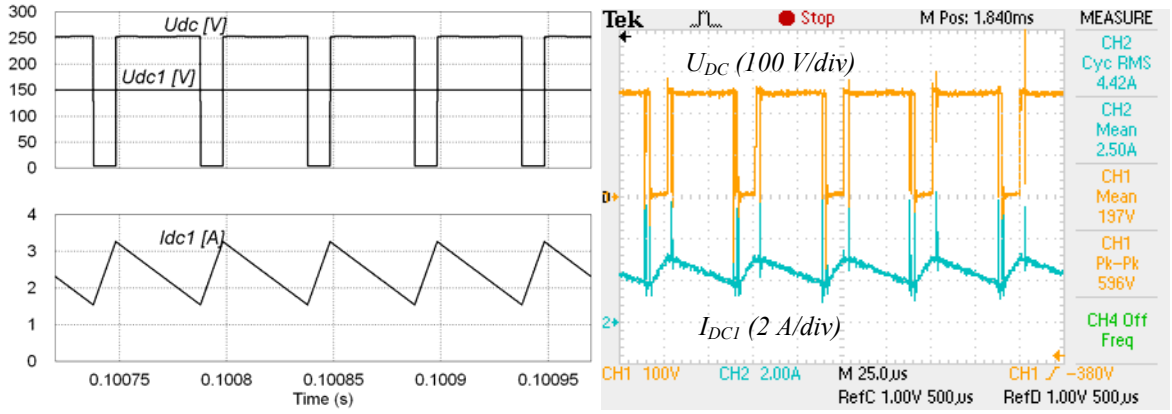
a) b)

Fig. 2.26. DC link voltage and input current at cut-in conditions



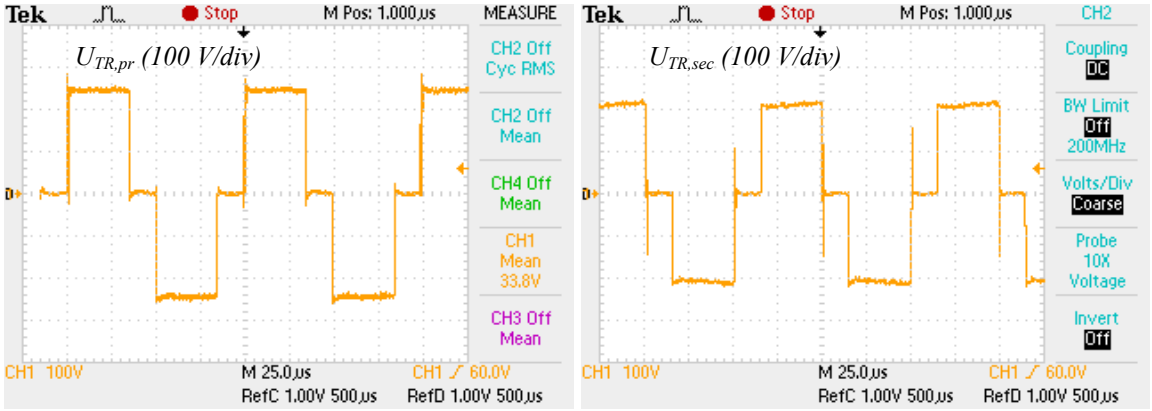
a) b)

Fig. 2.27. Voltages of transformers primary and secondary windings



a) b)

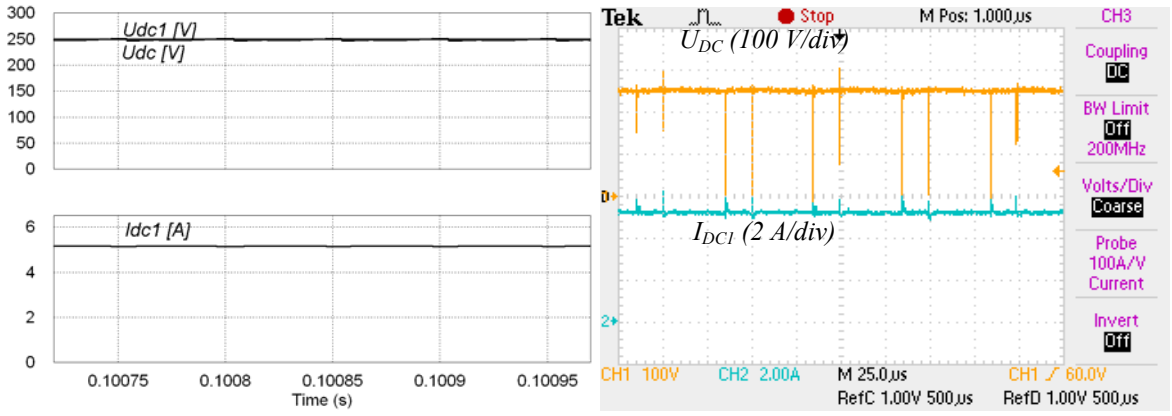
Fig. 2.28 . DC link voltage and input current at rated speed conditions (330 W)



a) b)

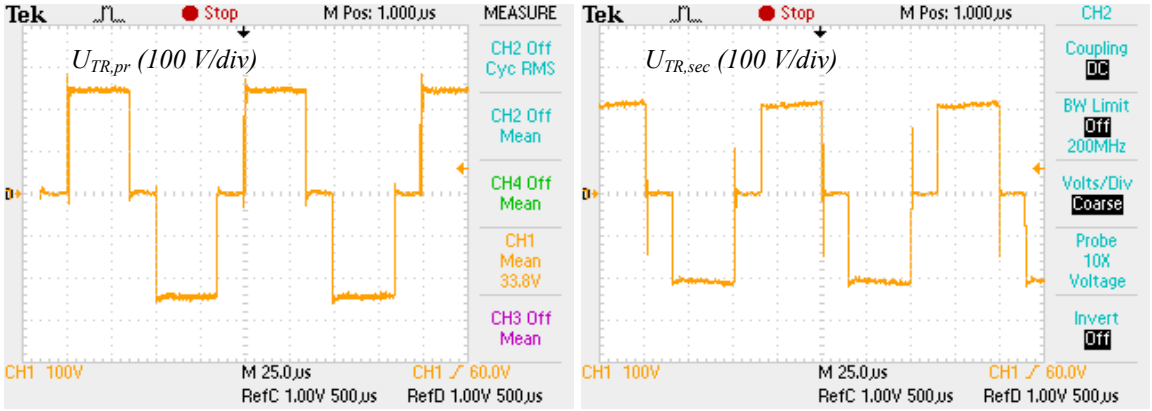
Fig. 2.29. Voltages of transformers primary and secondary windings

The third test was performed at the maximum generator-side DC link voltage (U_{DC1} = 250 V), which corresponds to the maximal power of the turbine (1250 W). At this operating point, when the input voltage equals the desired intermediate DC-link voltage (U_{DC1} = U_{DC} = 250 V), the shoot-through states were eliminated (D_S = 0) and the converter operated as a traditional VSI (Fig. 2.30.). In that case the isolation transformer is supplied with voltage pulses with the amplitude value equal to the generator-side DC link voltage. The voltage waveforms of the isolation transformer in this operation point are similar to those presented in Fig. 2.31.



a) b)

Fig. 2.30. DC link voltage and input current at rated wind speed (1250 W)



a) b)

Fig. 2.31. Voltages of transformers primary and secondary windings

2.3. Control methods of qZS inverters

This chapter unveils three shoot-through PWM control methods for the proposed DC/DC converter: shoot-through by the overlap of active states, shoot-through during freewheeling states and shoot-through during zero states [58]. The shoot-through states are evenly spread over the switching period so that the number of higher harmonics in the transformer could be reduced. In order to reduce switching losses of the transistors, the number of shoot-through states per period was limited by two. Moreover, in order to evenly distribute conduction and switching losses of transistors both inverter legs are involved in the shoot-through operation.

2.3.1. Shoot-through by overlapping of active states.

Fig. 2.32. presents the control principle of the single-phase qZSI where the shoot-through states are created by the overlap of active states, as shown in Fig. 2.32a and Fig. 2.32b. It is remarkable that the inverter can operate without dead time. In this case the duty cycle of active states of transistors is greater than or equal to 0.5. If active state duty cycle is greater than 0.5 overlapping of active states of transistors occurs and the shoot-through states are created (Fig. 2.32). During this operating mode the current through inverter switches increases, the voltage across the inverter bridge (U_{DC}) drops to zero (Fig. 2.32c). The resulting voltage waveform of the isolation transformer is presented in Fig. 2.32d.

The operating period of the isolation transformer in this control method consists of a shoot-through state t_S and an active state t_A:

$$T = t_A + t_S . \tag{54}$$

The (55) could also be represented as

$$\frac{t_A}{T}+\frac{t_S}{T}=D_A+D_S=1, \tag{55}$$

where D_A - is the duty cycle of active state;

D_S - is the duty cycle of shoot-through state.

As it is seen from Eq. (55) and also from Fig. 2.32d the duty cycle of active state will vary with the variation of the shoot-through duty cycle. It approaches its maximum in the non-shoot-through mode, when the input voltage is high enough and the shoot-through states are eliminated. And vice versa, in conditions of minimal input voltage where the shoot-through duty cycle is maximal the duty cycle of active states will have a minimum value. It should also be noted that for the voltage fed applications with the positive input voltage the maximum shoot-through duty cycle should never exceed 0.5 or the system could get instable. From practical point of view the shoot-through duty cycles longer than 0.3 are not advisable due to the rapid increase of losses.

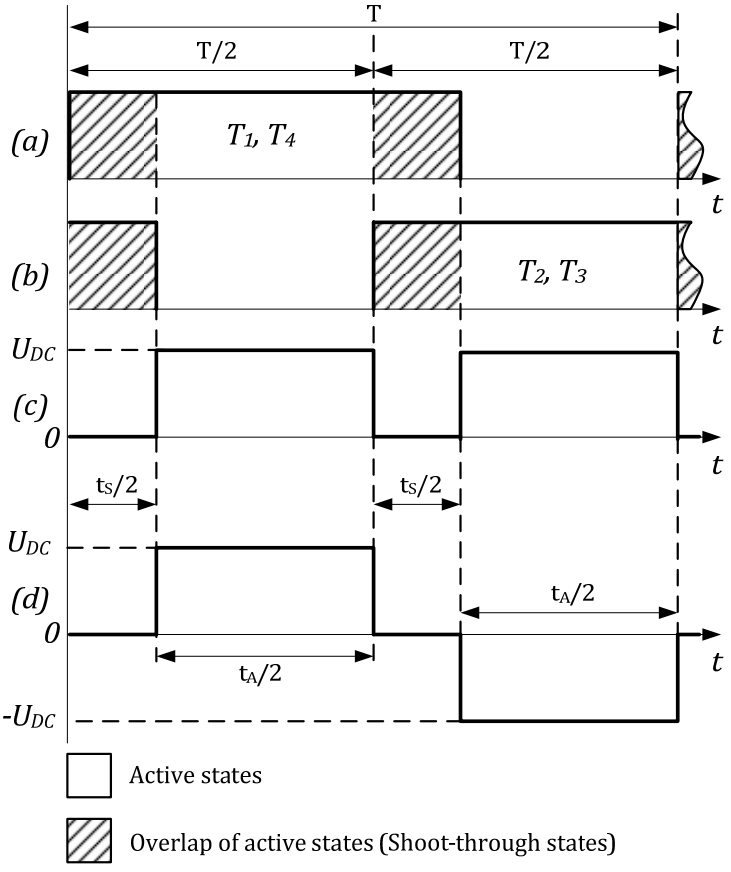


Fig. 2.32. Principle of shoot-through generation by the overlap of active state

Active and shoot-through states are controlled by two 180 phase shifted PWM signal generators operating with constant frequency and variable duty cycle ($D \geq 0.5$ for each generator). The simulation results (Fig. 2.33.) of this control methodology performed at minimal input voltage $U_{IN,min}$=150 V and the shoot-through duty cycle D_S=0.2 shows that the qZSI ensures the demanded voltage gain (B_{max}=1.66). The operating frequency of the impedance network is twice the operating frequency of the isolation transformer, while the switching frequency of power transistors is the same as transformer's one.

Despite the overall simplicity of this control methodology the direct dependency between duty cycles of active and shoot-through states could sometimes be problematic e.g. in the case of full-bridge output rectifier where active state duty cycle is used for output voltage compensation and the shoot-through duty cycle controls only the DC-link voltage. This means that the duty cycles should be independently controllable. Following two shoot-through PWM control methods can solve that problem.

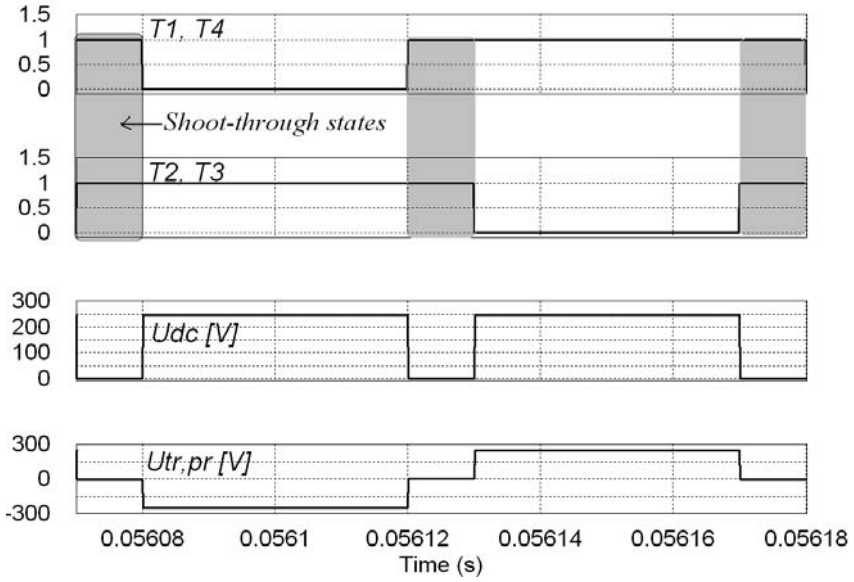


Fig. 2.33. Gating signals of transistors ($T_1 \ldots T_4$), DC-link voltage (U_{DC}) and resulting primary voltage of the isolation transformer ($U_{TR,pr}$)

2.3.2. Shoot-through during freewheeling states

One of possible solutions to control the active and shoot-through states separately is to arrange shoot-through states during freewheeling states where all the inverter switches are turned off (Fig. 2.34.).

For proper operation the freewheeling time t_{FRW} should meet the following condition:

$$t_{FRW} \geq t_{S,\max}, \tag{56}$$

where $t_{S,\max}$ - is the maximum duration of the shoot-through states per one switching period.

In the current control method the operating period of the isolation transformer consists of an active state t_A, a shoot-through state t_S and a freewheeling state t_{FRW}:

$$T = t_A + t_{FRW} \tag{57}$$

Equation (57) could also be represented as:

$$\frac{t_A}{T} + \frac{t_{FRW}}{T} = D_A + D_{FRW} = 1, \tag{58}$$

where D_A - is the duty cycle of active state;

D_{FRW} - is the duty cycles of freewheeling state.

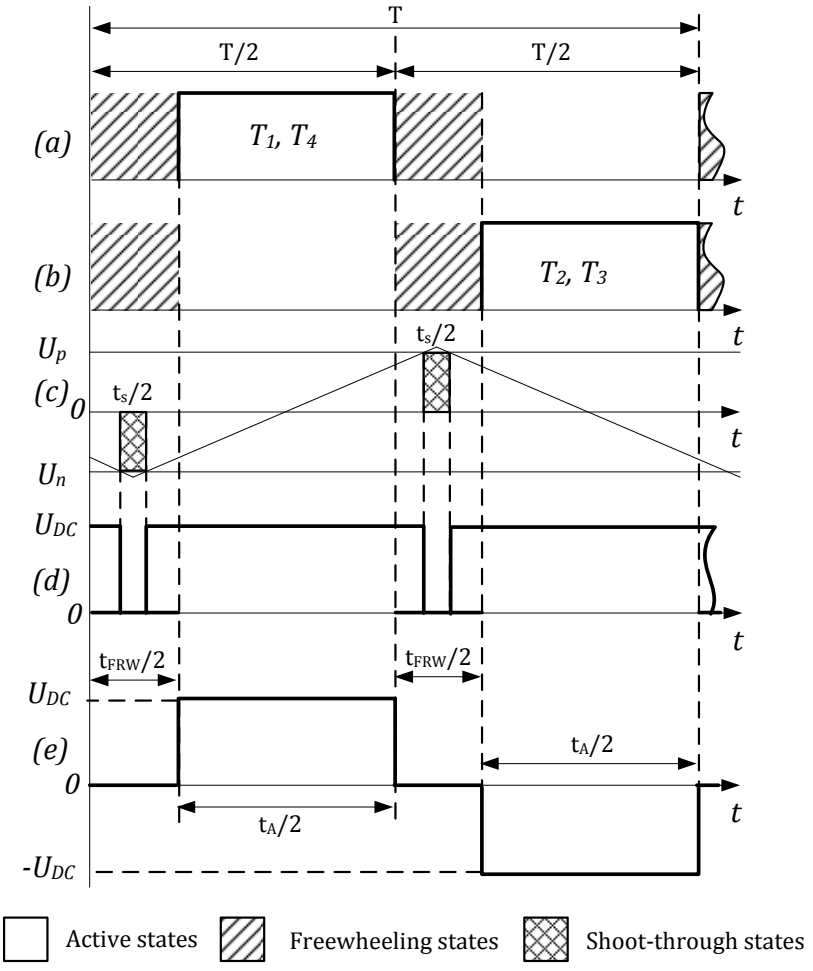


Fig. 2.34. Principle of shoot-through generation during freewheeling state

The duty cycle of active states remains unchanged despite the fluctuation on the input voltage and on the shoot-through duty cycle.

Fig. 2.34. illustrates the control methodology and resulting voltages of the single-phase qZSI with the shoot-through states arranged during freewheeling states. The block diagram of the gating signal generator for the proposed control method is shown in Fig. 2.35. It involves two parts: an active and a shoot-through state control. Active states are controlled by two 180 phase shifted PWM signal generators (PWM1 and PWM2) operating with constant frequency and duty cycle. The transistors are driven alternately in pairs (T_1 and T_4, then T_2 and T_3). The shoot-through states are generated using a triangle waveform generator and two comparators. When the modulation waveform is greater than the value of the reference signal U_p, the first shoot-through state (all the transistors turned on) appears and when the modulation signal is smaller than the reference signal U_n, the second shoot-through state takes the place.

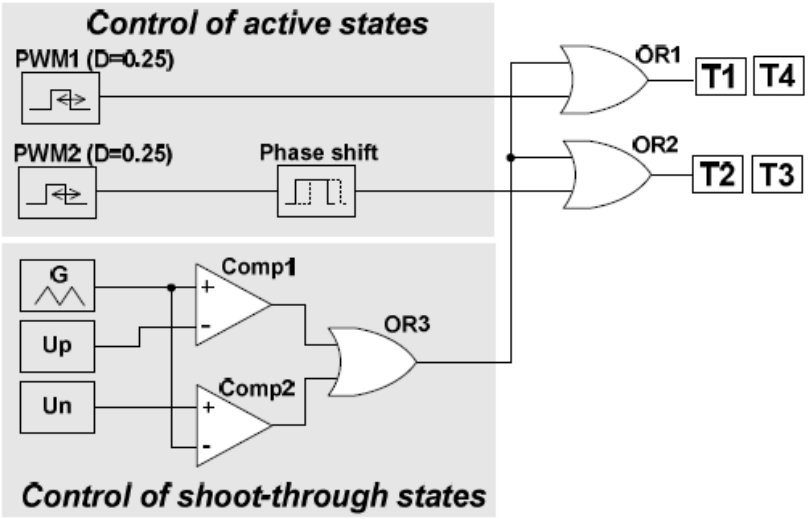


Fig. 2.35. Principle of shoot-through generation during freewheeling states

Simulations of this control method (Fig. 2.36) performed at minimal input voltage $U_{IN,min}$=150 V, D_S=0.2, active state duty cycle of the isolation transformer D_A=0.7 and duty cycle of freewheeling states D_{FRW}=0.3 show that the qZSI ensures the demanded voltage gain (B_{max}=1.66). The operating frequency of the impedance network is twice the operating frequency of the isolation transformer, while the switching frequency of power transistors is three times higher than that of isolation transformer. In the case of high input voltage when the shoot-through states are eliminated the transistors operate with the same frequency as isolation transformer.

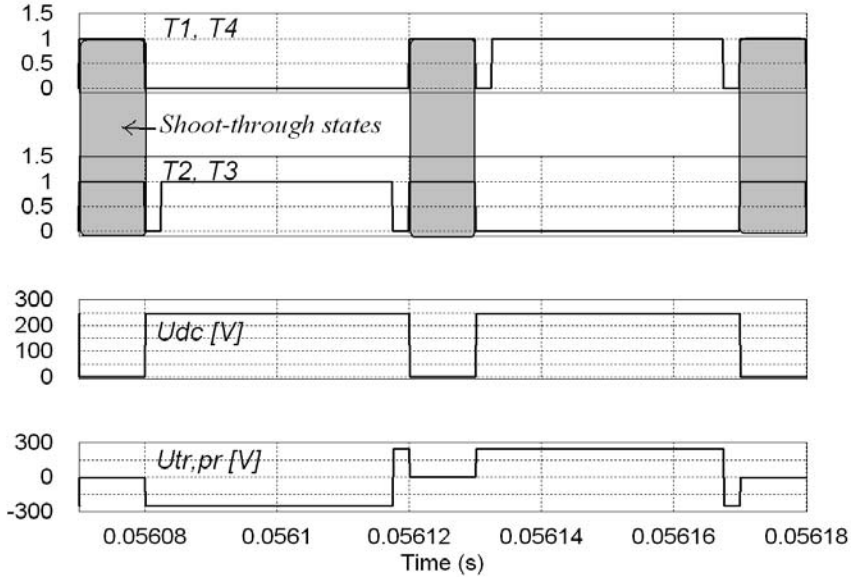


Fig. 2.36. Gating signals of transistors ($T_1 \ldots T_4$), DC-link voltage (U_{DC}) and resulting primary voltage of the isolation transformer ($U_{TR,pr}$)

2.3.3. Shoot-Through During Zero States

As an alternative, the freewheeling states in the control methodology could be replaced by the classic zero states when the primary winding of the isolation transformer is shorted through either the top (T_1 and T_3) or bottom (T_2 and T_4) inverter switches. The block diagram of gating signal generator for this control methodology is presented in Fig. 2.37.

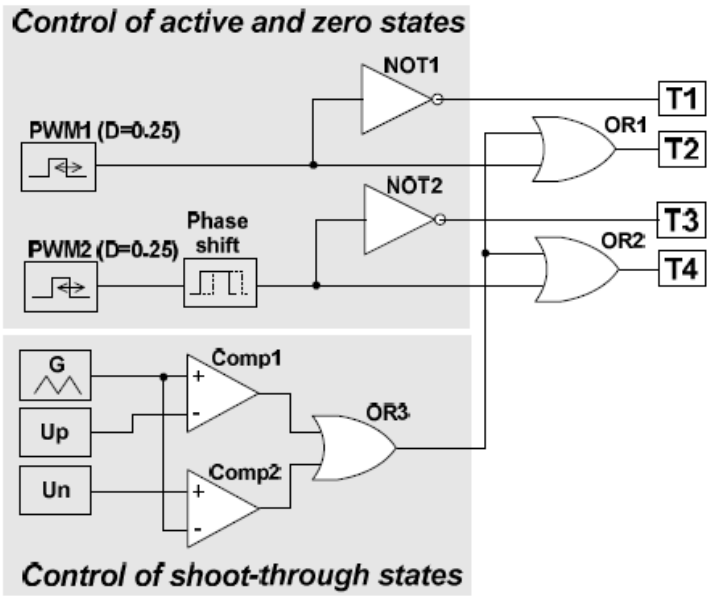
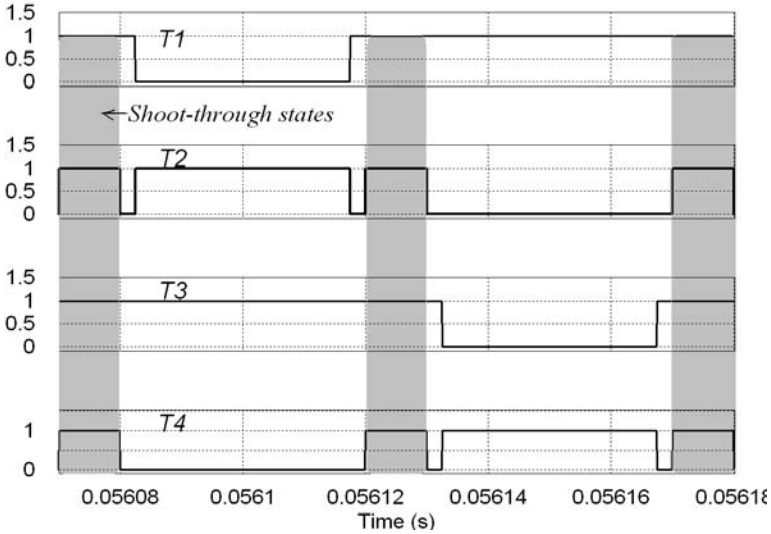


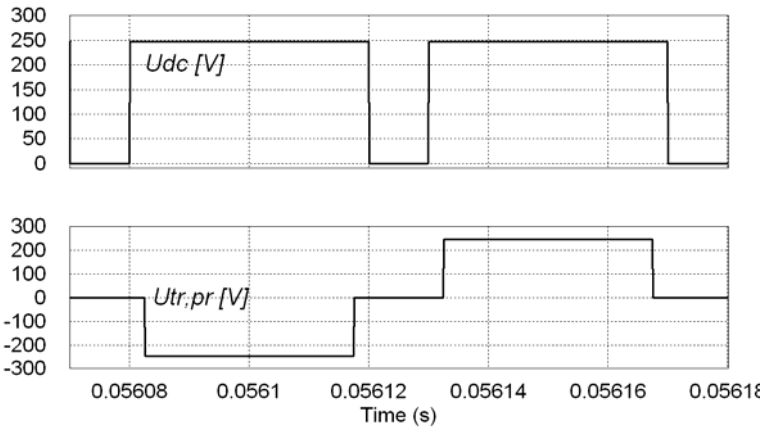
Fig. 2.37. Principle of shoot through generation during zero states

Active states are controlled by two 180 phase shifted PWM signals. The signals for upper transistors T_1 and T_3 are inverted. The shoot-through states are generated using a triangle waveform generator and two comparators.

Simulations of this control method (Fig. 2.38) performed at minimal input voltage $U_{IN,min}$=150 V, D_S=0.2, duty cycle of active states D_A=0.7 and duty cycle of zero states D_Z=0.1 show that the qZSI ensures the demanded voltage gain (B_{max}=1.66). It is seen, that the zero states are produced by the simultaneous conduction of top-side transistors (T_1 and T_3). In this control algorithm the switching frequency of the top-side transistors in the shoot-through mode is equal to the operating frequency of the isolation transformer, while the switching frequency of the bottom-side transistors (T_2 and T_4) is three times higher than that of T_1 and T_3. In the case of high input voltage when the shoot-through states are eliminated the transistors operate with the same frequency as isolation transformer.



a)



b)

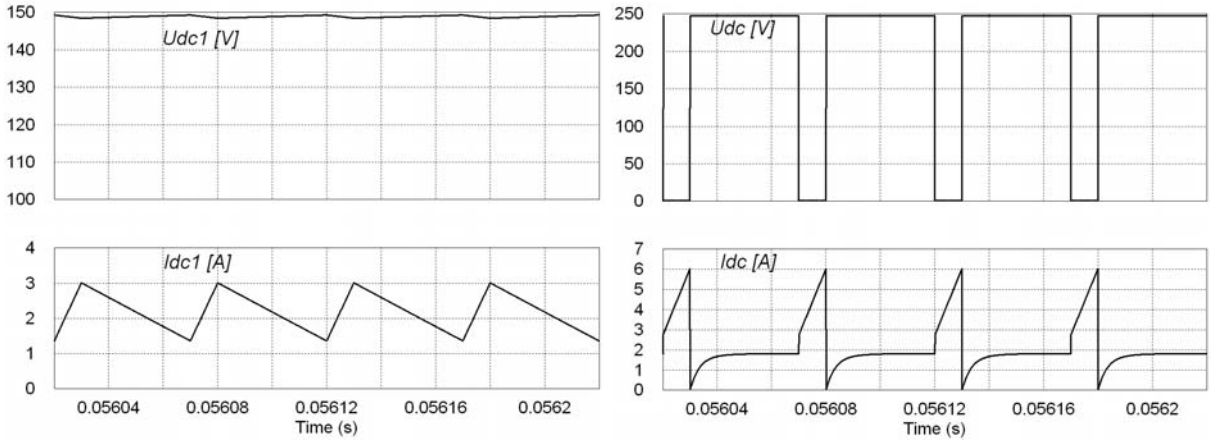
Fig. 2.38. Gating signals of transistors (T1…T4) a) and DC-link voltage (U_{DC}) and resulting primary voltage of the isolation transformer ($U_{TR,pr}$) b)

2.3.4. Simulation results

The PSIM model of the qZSI-based single-phase DC/DC converter was developed and simulations made to analyse the three [58] control algorithms. For all simulations the input voltage of the converter was set to U_{DC1}=150 V and the output power was P=330 W (rated conditions). Other operating parameters and values were selected in accordance with design specifications presented in Table 2.4. The input voltage, input current, collector-emitter voltages and collector currents of transistors from one inverter leg as well as primary winding waveforms of isolation transformer and voltage profiles of the capacitors in qZS-network were measured.

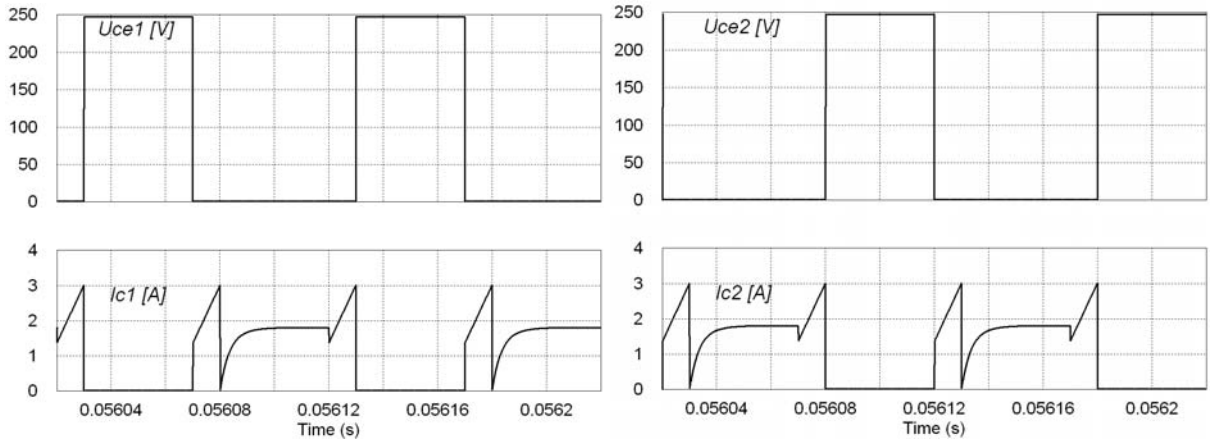
Shoot-Through by the Overlap of Active State

Operating waveforms of the single-phase qZSI associated with the shoot-through control method by the overlap of active states are presented in Fig. 2.39. - Fig. 2.41. The duty cycles of the active and shoot-through states are 0.7 and 0.2 for one operating period, respectively. The qZSI ensures continuous input current (Fig. 2.39.a) and the demanded input voltage gain (Fig. 2.39.b). It is seen from the Fig. 2.40. that the top - and the bottom side transistors operate with the same switching frequency and have the similar operating waveforms.



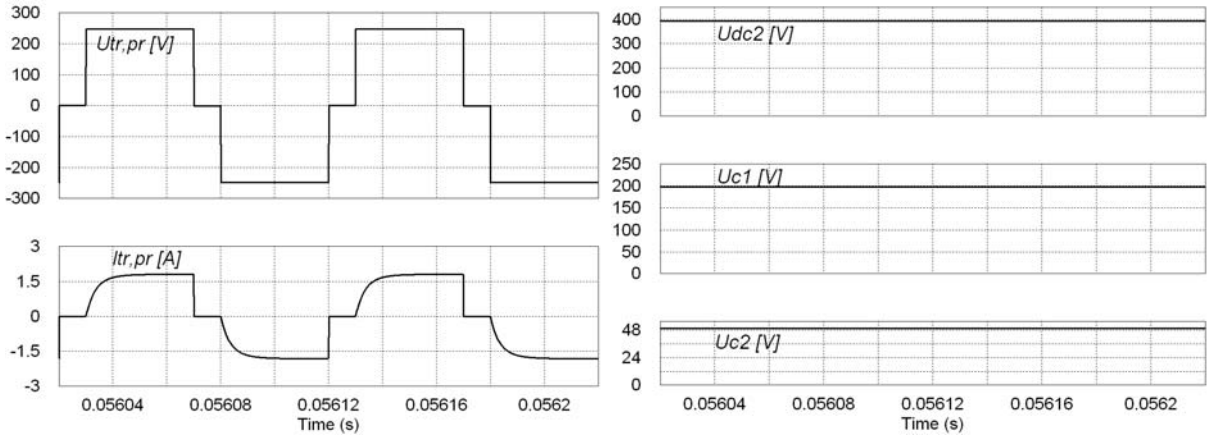
a) b)

Fig. 2.39. Waveforms of input voltage (U_{DC1}) and current (I_{DC1}) (a) and DC-link voltage (U_{DC}) and current (I_{DC}) (b)



a) b)

Fig. 2.40. Waveforms of collector-emitter voltage (U_{ce}) and collector current (I_c) of top-side transistor T_1 (a) and bottom-side transistor T_2 (b)



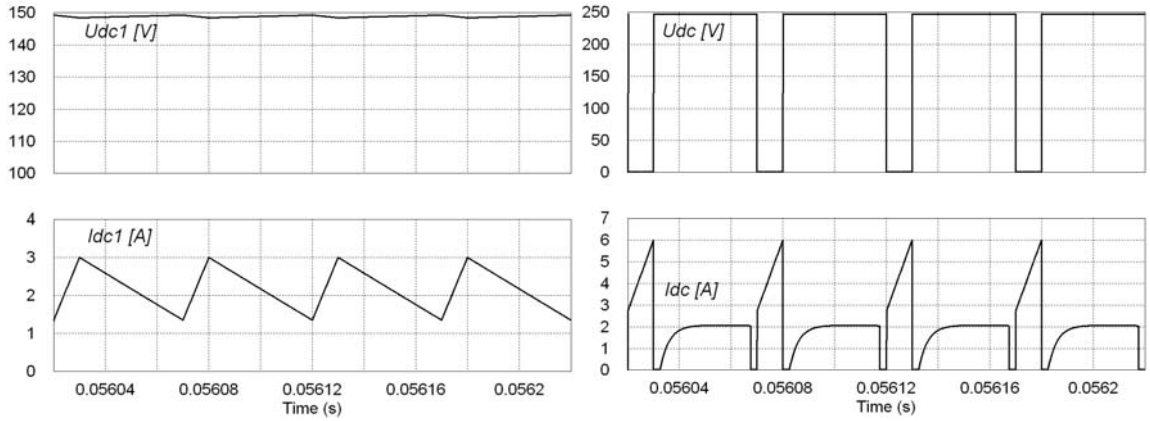
a) b)

Fig. 2.41. Waveforms of primary voltage ($U_{tr,pr}$) and current ($I_{tr,pr}$) of the isolation transformer (a) and voltage profiles of grid side DC link voltage (U_{DC2}) and capacitor voltages C_1 and C_2 (U_{C1}, U_{C2}) of the qZS-network (b)

Shoot-Through During Freewheeling State

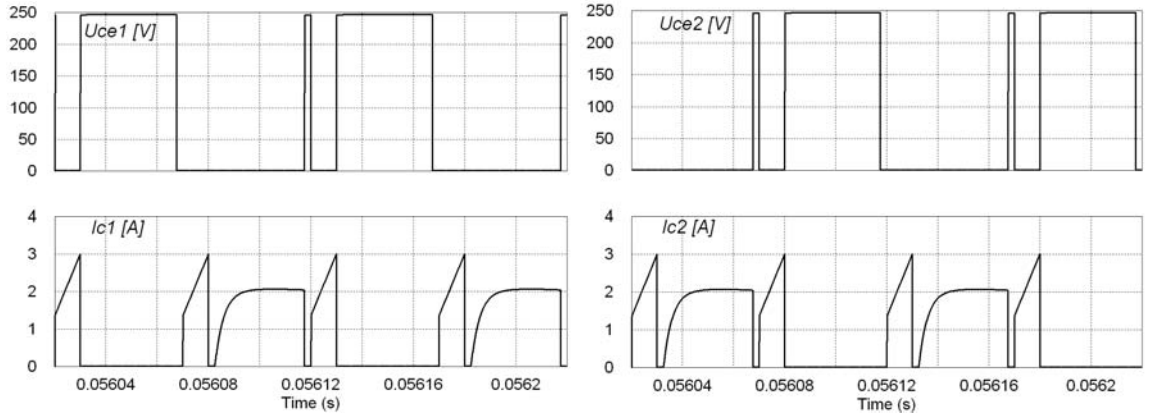
Operating waveforms of the single-phase qZSI associated with the shoot-through PWM control method where the shoot-through states are generated during freewheeling states of the inverter are presented in Fig. 2.42. - Fig. 2.44. The duty cycles of the active, freewheeling and shoot-through states are 0.7, 0.3 and 0.2 for one operating period, respectively. The qZSI ensures continuous input current (Fig. 2.42.a) and the demanded input voltage gain (Fig. 2.42.b). As it is seen from the Fig. 2.43., the top - and the bottom-side transistors operate with the same switching frequency and have similar operating waveforms.

The transistors are partially soft switched. Zero voltage switching is achievable for both top - and bottom-side transistors, as indicated in Fig. 2.43.



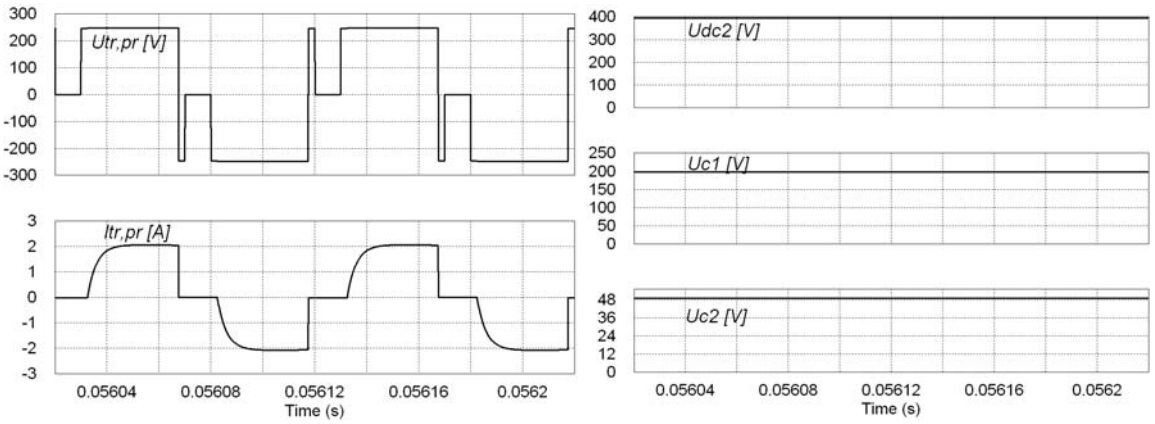
a) b)

Fig. 2.42. Waveforms of input voltage (U_{DC1}) and current (I_{DC1}) (a) and DC-link voltage (U_{DC}) and current (I_{DC}) (b)



a) b)

Fig. 2.43. Waveforms of collector-emitter voltage (U_{ce}) and collector current (I_c) of top-side transistor T_1 (a) and bottom-side transistor T_2 (b)

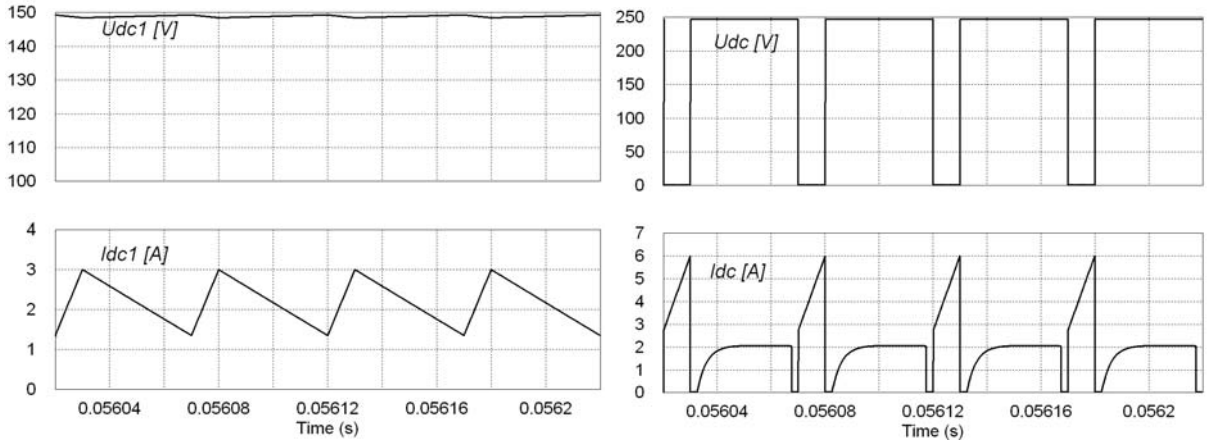


a) b)

Fig. 2.44. Waveforms of primary voltage ($U_{tr,pr}$) and current ($I_{tr,pr}$) of the isolation transformer (a) and voltage profiles of grid side DC link voltage (U_{DC2}) and capacitor voltages C_1 and C_2 (U_{C1}, U_{C2}) of the qZS-network (b)

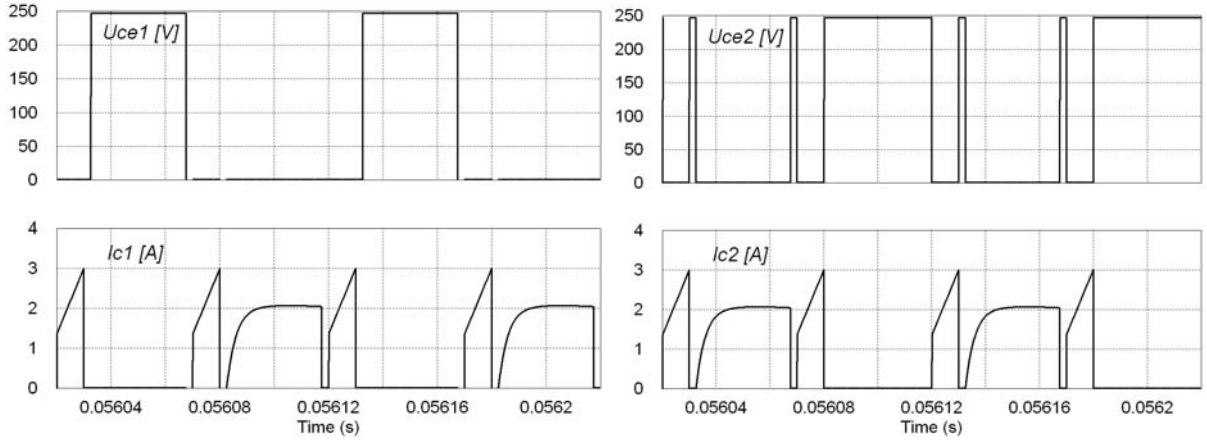
Shoot-Through During Zero State

Operating waveforms are presented in Fig. 2.45-Fig. 2.46. The duty cycles of the active, zero and shoot-through states of the isolation transformer are 0.7, 0.3 and 0.2 for one operating period, respectively. The operating currents of power switches as well as the profile of the DC-link current are similar to those of previous control method. Benefit of the given control methodology is that due to introduction of zero states instead of freewheeling states the undesired spikes caused by the leakage inductance of the isolation transformer were fully eliminated [58]. It is remarkable that full soft switching without additional components is achieved for top-side transistors (T_1 and T_3), as shown in Fig. 2.46.a.



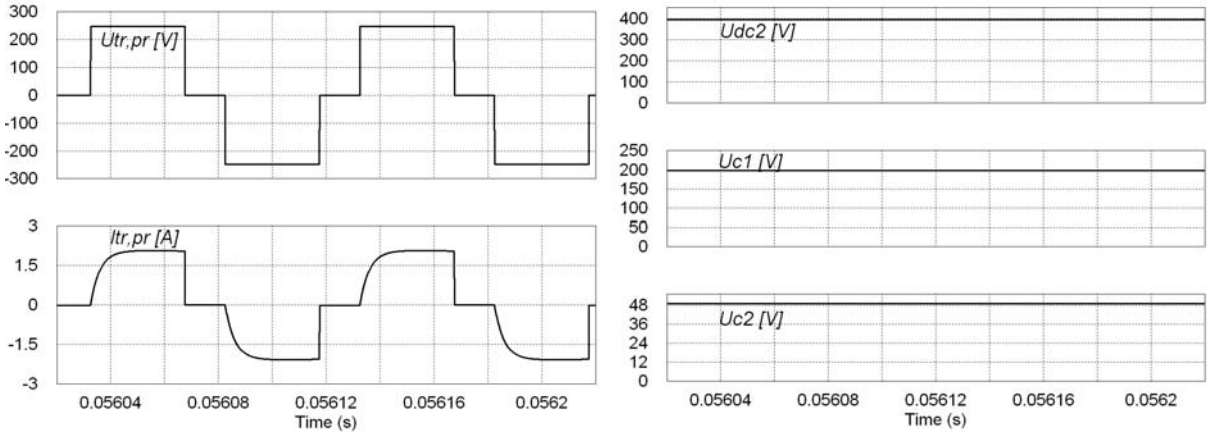
a) b)

Fig. 2.45. Waveforms of input voltage (U_{DC1}) and current (I_{DC1}) (a) and DC-link voltage (U_{DC}) and current (I_{DC}) (b)



a) b)

Fig. 2.46. Waveforms of collector-emitter voltage (U_{ce}) and collector current (I_c) of top-side transistor T_1 (a) and bottom-side transistor T_2 (b)



a) b)

Fig. 2.47. Waveforms of primary voltage ($U_{tr,pr}$) and current ($I_{tr,pr}$) of the isolation transformer (a) and voltage profiles of grid side DC link voltage (U_{DC2}) and capacitor voltages C_1 and C_2 (U_{C1}, U_{C2}) of the qZS-network (b)

2.3.5. Comparison of Shoot-Through PWM Control Method

The operating values of the qZSI-based isolated DC/DC converter operating in voltage boost (shoot-through) mode and with different shoot-through PWM control methods are presented and compared in Table 2.5. The compared shoot-through PWM control methods are designated as „A", „B" and „C" for the shoot-through by the overlap of active states, shoot-through during freewheeling states and shoot-through during zero states, respectively.

Table 2.5

Comparison of shoot-through PWM control methods

Parameter	Method "A"	Method "B"	Method "C"
Operating frequency of the qZS-network during shoot-through	$2 \cdot f_{TR}$	$2 \cdot f_{TR}$	$2 \cdot f_{TR}$
Minimal switching frequency of top-side transistors	f_{TR}	f_{TR}	f_{TR}
Maximal switching frequency of top-side transistors	f_{TR}	$3\ f_{TR}$	f_{TR}
Minimal switching frequency of bottom side transistor	f_{TR}	f_{TR}	f_{TR}
Maximal switching frequency of bottomside transistors	f_{TR}	$3\ f_{TR}$	$3\ f_{TR}$
Soft switching for top-side transistor	no	partially	full
Soft switching for bottom-side transistor	no	partially	no

It can be seen that the modulation method “A” has the most optimal operating parameters. The switching frequencies of transistors are the smallest and are equally distributed between all switches. However, the method utilizes active states overlapping to generate the shoot-through states, which inherently connects shoot-through and active state duty cycles such that they cannot be changed separately. In cases were such method is unacceptable the modulation method “B” or “C” can be implement. In general, method “C” seems to be a better choice since it has reduced switching frequency of the top-side transistors and according to [58] have lower overvoltages and it provides no leakage inductance spikes in the transformer voltage. Moreover, the top-side transistors are fully soft switched.

2.4. Interface converter for micro turbines

To reduce the overall cost of the system and taking into account “overbost” effect of qZS DC/DC converter was offered simplified interface converter (Fig. 2.32.). Elimination of controlled rectifier allows utilization of simpler control circuit. Since there is no need for input voltage and current sensing anymore the overall cost of converter is significantly lower.

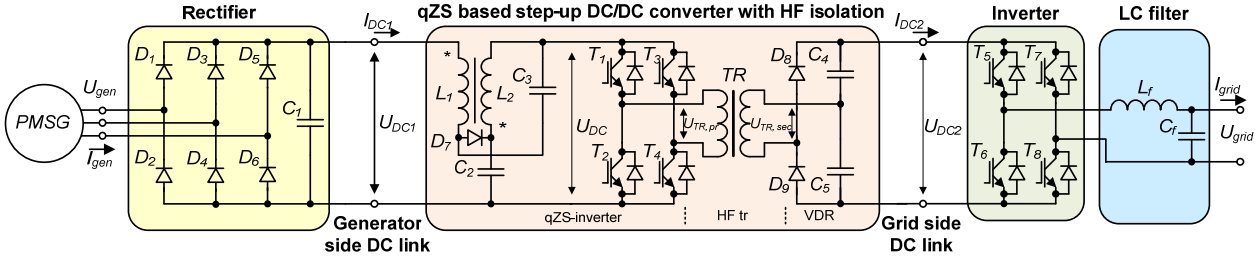


Fig. 2.48. Power circuit for wind turbine systems of micro power level

The controlled rectifier is substituted with uncontrolled one to reduce the number of switches and simplify the control circuitry. The necessary boost is obtained only by qZS DC/DC converter. Converter operation modes at different wind speeds for the particular application with 1.3 kW PMSG are illustrated in Fig. 2.49.

First, the rectifier converts the variable voltage with the variable frequency U_{gen} from the PMSG into a DC voltage U_{DC1}. The generator side DC link voltage range is between 70 V at cut-in conditions and 250 V in constant speed mode.

The qZS based step-up DC/DC converter is stabilizing the grid-side DC link voltage U_{DC2} at 400 V DC despite the variation of the generator-side DC link voltage U_{DC1} in the range from 150 V to 250 V. Neglecting losses in components, the output voltage of the qZS based step-up

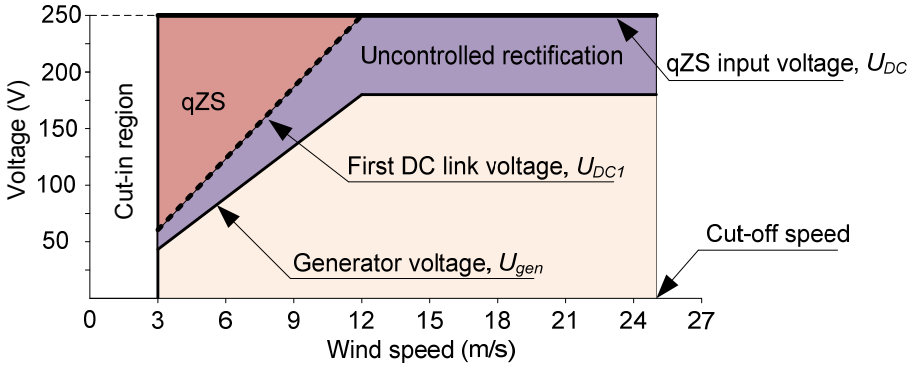


Fig. 2.49. Operation modes of the simplified interface converter

DC/DC converter operating in the continuous conduction mode (CCM) could be estimated as

$$U_{DC2} = \frac{2 \cdot U_{DC1}}{n} \cdot \left(\frac{1}{1 - 2 \cdot D_S} \right), \tag{59}$$

where U_{DC1} - is the generator-side DC link voltage;

n - is the turns ratio of the primary and secondary windings of the isolation transformer;

D_S - is the shoot-through duty cycle.

The shoot-through is a special operation state of the qZS based step-up DC/DC converter, when the primary winding of the isolation transformer is shorted through both the upper and lower switches of all two phase legs. The unique qZS-network (see Fig. 2. 33). makes the shoot-through states possible, effectively protecting the circuit from damage. Moreover, the shoot-through states are used to boost the magnetic energy stored in the DC-side inductors L_1 and L_2 without short-circuiting the DC capacitors C_2 and C_3. This increase in the inductive energy in turn provides the boost of the voltage seen on the inverter output during the active states of the inverter. In that way, by keeping the voltage U_{DC} constant the inverter could be operated with a fixed duty cycle value, thus ensuring constant volt-second and flux swing of the isolation transformer TR.

As it is seen from Fig. 2.48. the proposed qZS-inverter has the input inductor *L1* that buffers the source current. It means that in the CCM the input current never drops to zero during the shoot-through states. However, in the case of small loads, relatively low switching frequency and low inductance values of *L1* and *L2*, the qZS-inverter could start to operate in the discontinuous conduction mode (DCM) and the input current falls to zero during some part of the switching period. In the current application, similar conditions could appear during

the operation of a wind turbine near the cut-in region, when the PMSG power drops to minimum.

The operating period of the qZS-inverter in the DCM generally consists of an active state t_A, a shoot-through state t_S and a discontinuous conduction state t_D

$$\frac{t_A}{T}+\frac{t_S}{T}+\frac{t_D}{T}=D_A+D_S+D_D=1, \tag{60}$$

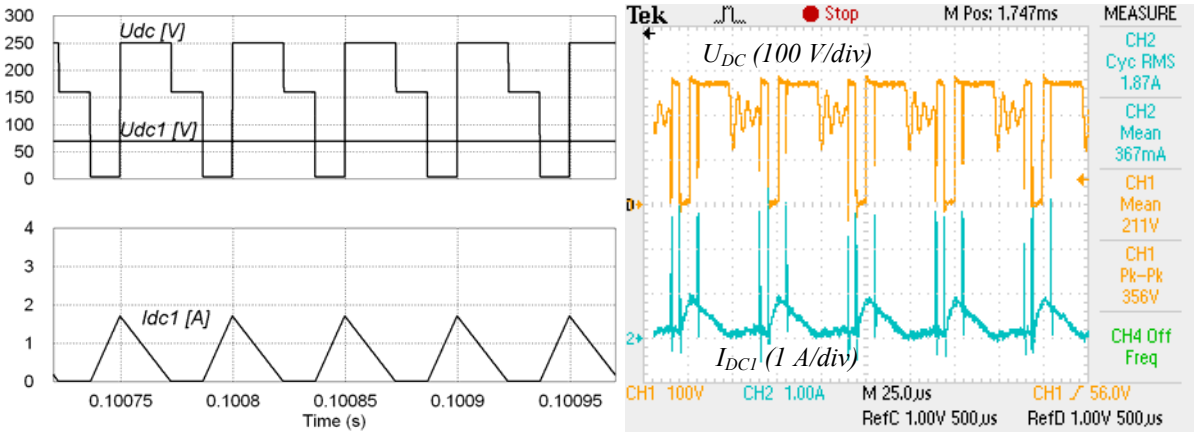
where D_A, D_S and D_D are the duty cycles of active, shoot-through and discontinuous conduction states, respectively.

In contrast to the CCM the operating voltage of the capacitor *C2* during the DCM will increase and it will lead to an increased peak value of the DC link voltage during the DCM, causing the "overboost effect" of the input voltage:

$$\hat{U}_{DC(DCM)}=U_{C2}+U_{C3}=\frac{1-D_D}{1-2\cdot D_S-D_D}\cdot U_{DC1}, \tag{61}$$

The PWM shoot-through control technique [86] was implemented during the tests. The qZS network was operating at 20 kHz frequency, but isolation transformer at 10 kHz.

In the first test the generator-side DC link voltage was set to 70 V that corresponds to the cut-in wind speed conditions. The load that corresponds to the turbine power at cut-in is 40 W. The qZS based DC/DC converter operates in the discontinuous conduction mode (DCM) at such load. The shoot-through duty cycle D_S was set at 0.27 for this mode. Peak DC link voltage U_{DC} is 250 V (Fig. 2.50.) that corresponds to theoretical assumptions stated in. The DCM for low power operation was chosen to reduce the size of the inductors. Due to long current paths in the laboratory prototype of the qZS based DC/DC converter that leads to parasitic inductances, the voltage oscillations can be observed at zero input current intervals.



a) b)

Fig. 2.50. Simulation a) and experimental b) results of simplified interface converter

2.5. Conclusions

The study of the wind theory shows that a VSWT allows maximum power from air flow to be extracted. PMSG based VSWT characteristics and wind properties on the Baltic coastal regions were analyzed to define the converter operation modes and. Converter topologies studied earlier shows that they are not well suited for micro VSWT applications due to the complexity and efficiency concerns

For these reasons the simplified topology of PMSG based VSWT and grid interfacing converter is presented in this paper. The converter consists of a rectifier, a quasi-Z-source DC/DC converter, a high frequency isolation transformer and a voltage doubler rectifier. Such topology offers necessary voltage boost properties and a simple power circuit. The results of performance tests demonstrate the interface converter ability to ensure the required grid side DC link voltage at all operation modes of PMSG-based WSVT. This topology could be implemented in residential PMSG VSWT applications with power up to 3kW

3. QZS DC/DC CONVERTER WITH IMPROVED BOOST PROPERTIES

This chapter proposes a possibility for further improvement of the quasi-Z-source based back-to-back interface converter by the introduction of the switched inductor quasi-Z-source network (Fig. 3.1.). In contrast to converters presented in Fig. 2.1. the new topology offers the increased voltage boost capability of the grid-side inverter.

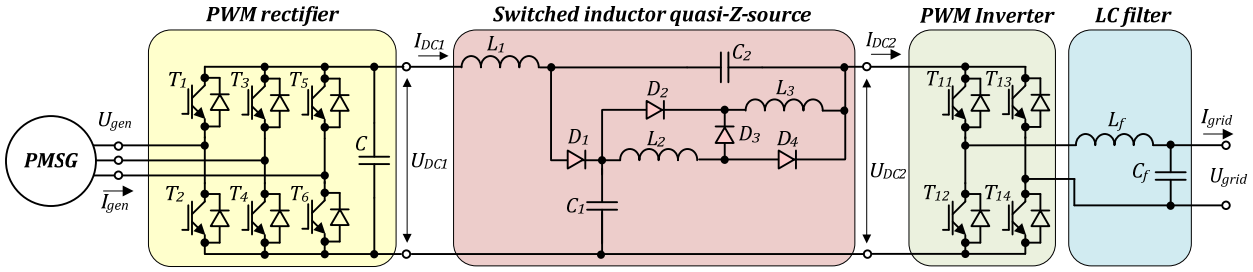


Fig. 3.1. New proposed switched inductor quasi-Z-source based back-to-back converter for VSWTs with PMSG

The proposed SL qZS network consists of three inductors ($L_1 \ldots L_3$), four diodes ($D_1 \ldots D_4$) and two capacitors (C_1 and C_2). Inductors L_2 and L_3 can be implemented as coupled inductors. Coupled with the grid side PWM inverter, the SL qZS network forms the SL quasi-Z-source inverter (SL qZSI). Similarly to the traditional qZSI [75], the SL qZSI has two main types of operational states at the DC side: non-shoot-through states and shoot-through states. Let us assume that the operating period T of the SL qZSI consists of a shoot-through state t_S and an active state t_A:

$$\frac{t_A}{T} + \frac{t_S}{T} = D_A + D_S = 1, \tag{62}$$

where D_A - is the duty cycles of an active state;

D_S - is the duty cycle of shoot-through state.

In order to simplify the analysis it was assumed that the capacitors, inductors and diodes of the SL qZS network are lossless. Fig. 3.2. shows the equivalent circuits of the SL qZSI operating in the CCM for the shoot-through (a) and active (b) states.

At the steady state the average voltage of the inductors over one operating period is zero:

$$U_{L1} = \int_{t}^{t+T} u_{L1} dt = 0;\ U_{L2} = \int_{t}^{t+T} u_{L2} dt = 0;\ U_{L3} = \int_{t}^{t+T} u_{L3} dt = 0. \tag{63}$$

Based on that fact and defining the shoot-through duty cycle as D_S and the non-shoot-through duty cycle as $(1\text{-}D_S)$, the inductors voltages over one operating period could be represented as

$$\begin{cases} U_{L1} = \overline{u}_{L1} = D_S(U_{DC1} + U_{C2}) + (1 - D_S)(U_{DC1} - U_{C1}) = 0 \\ U_{L2} = U_{L3} = \overline{u}_{L2} = \overline{u}_{L3} = D_S U_{C1} + (1 - D_S)(-\frac{U_{C2}}{2}) = 0 \end{cases}. \tag{64}$$

Equations for average capacitor voltages U_{C1} (4), U_{C2} (5) and peak inverter input voltage U_{DC2} (6) are derived from the steady state analysis.

$$U_{C1} = \frac{U_{DC1} \cdot (1 - D_S)}{(1 - 2 \cdot D_S - D_S^2)}. \tag{65}$$

$$U_{C2} = \frac{U_{DC1} \cdot 2 \cdot D_S}{(1 - 2 \cdot D_S - D_S^2)}. \tag{66}$$

$$\hat{U}_{DC2} = \frac{U_{DC1} \cdot (1 + D_S)}{(1 - 2 \cdot D_S - D_S^2)} = B \cdot U_{DC1}. \tag{67}$$

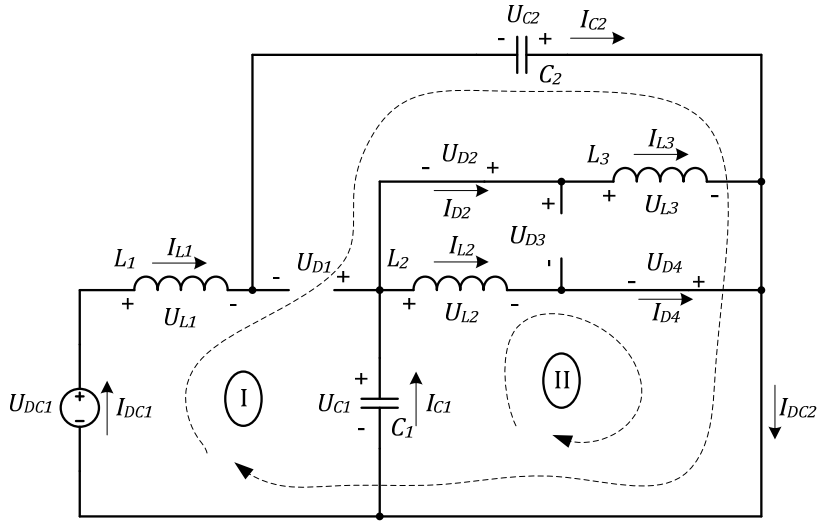
The voltage conversion ratio G of the whole inverter can be expressed by

$$G = \frac{U_{grid\,m}}{U_{DC1}} = M \cdot B, \tag{68}$$

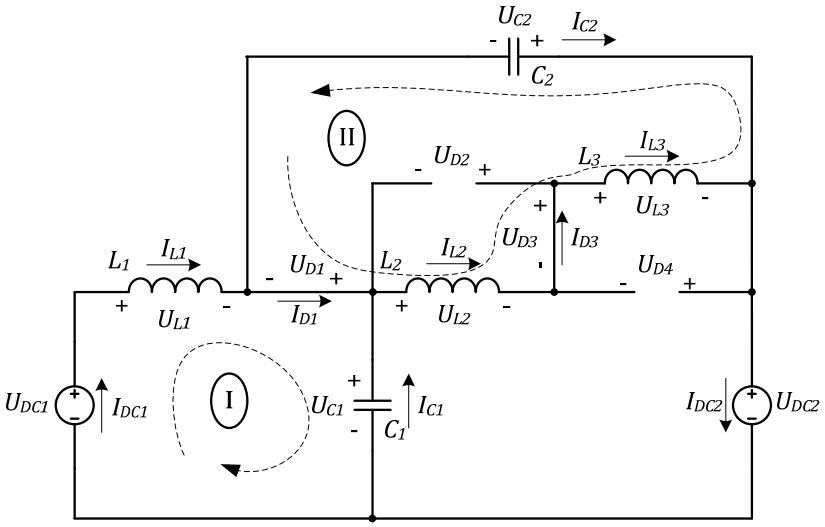
where M - is the modulation index.

The modulation index is connected with the shoot-through duty cycle by the following relation [2]:

$$M \le 1 - D_S, \tag{69}$$



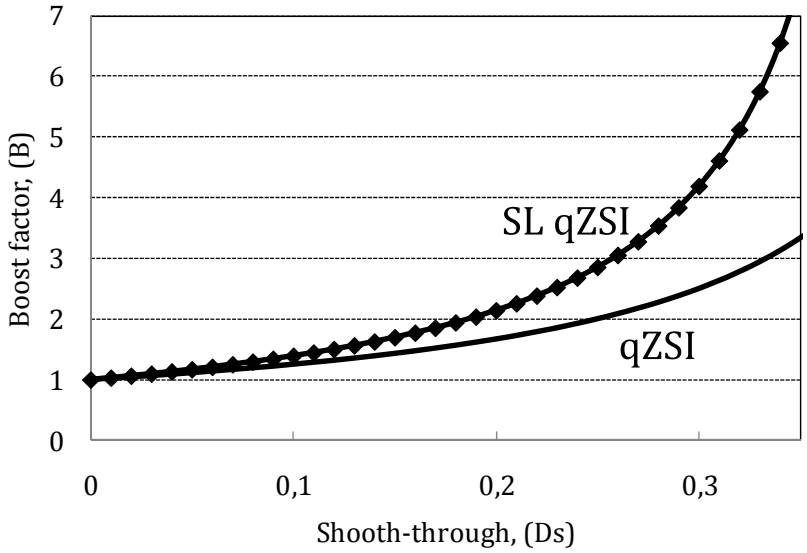
(a)



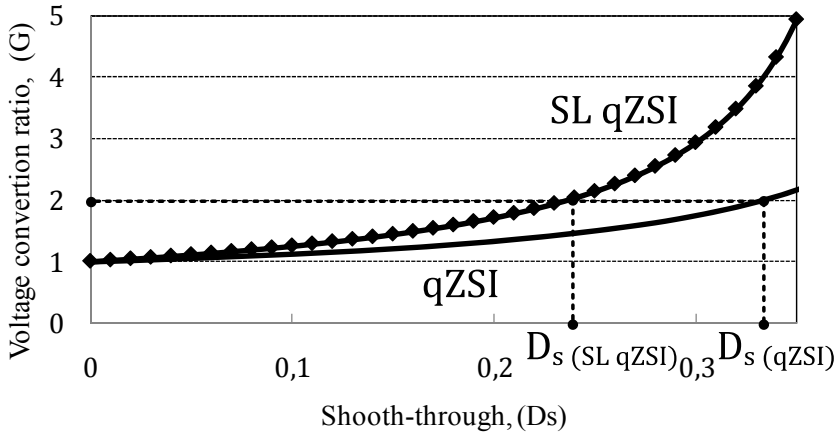
(b)

Fig. 3.2. Equivalent circuits of the SL qZSI: during shoot-through state (a) and during active (non-shoot-through) state (b)

In Fig. 3.3. the voltage boost factor B and the voltage conversion ratio G of the traditional qZSI are compared with those of the proposed SL qZSI. It is seen that the shoot-through duty cycle D_S for the SL qZSI is lower than for traditional qZSI at the same voltage conversion ratio G (Fig. 3.3.*b*). This is significant feature of the SL qZSI that allows expand the grid voltage regulation possibilities at reduced grid side DC link peak voltage U_{DC2p}.



(a)



(b)

Fig. 3.3. Boost factor *B* (a) and voltage conversion ratio *G* (b) as functions of the shoot-through duty cycle for qZSI andd SL qZSI

3.1. Operation modes of the interface converter

Generally, PMSG based VSWTs have three distinct operation modes: silent mode, variable speed operation mode and constant speed mode. A turbine is silent in two cases: wind speed is below a cut-in level or above the cut-off speed. Turbines operate at variable speed in the wind velocity range from cut-in to rated wind speed. Rated wind speed differs by turbine types, but often has the value of 12 meters per second. Constant speed mode takes place above the rated wind speed and output power of the turbine remains constant at this mode.

PMSG with 8 pole pairs was considered as a power source in this research. Its line voltage is 140 V at 375 rpm, but it can operate up to 510 rpm. This speed is considered as the maximum power operational point for the turbine and the generator. Generator power reaches 1250 W at this point with the output voltage of 183 V. Cut-in speed for a turbine is 125 rpm and it can produce 40 W, but the generator voltage is only 48 V at this point. So this is the lowest input voltage for an interface converter.

Based on the specifications of the PMSG the operation modes of the proposed back-to-back interface converter are presented in Fig. 8. The necessary voltage boost is obtained in two steps. The PWM rectifier stabilizes the DC link voltage U_{DC1} to a 150 V level when the generator voltage is below 112 V. This operation mode of the converter is called a PWM mode. The transferred power of the converter lies between 40 W and 330 W at this mode.

The controlled rectifier works as diode rectifier when the generator voltage U_{gen} is above 112 V. In this mode the DC link voltage is changed proportionally to the generator voltage, at the range from 150 V in rated generator speed conditions up to 250 V at the maximal speed.

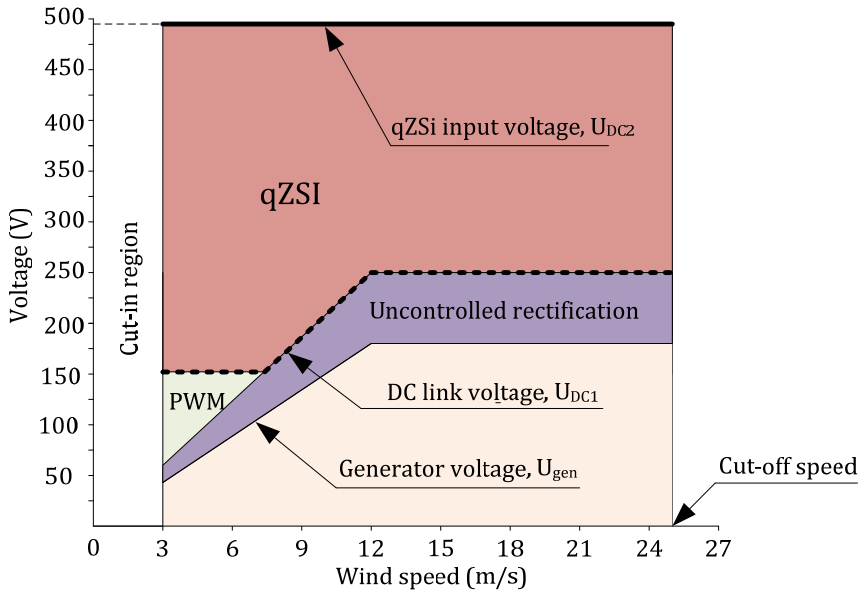


Fig. 3.4. Operation modes of the proposed converter

The SL qZS network with appropriate inverter control is stabilizing the peak value of the inverter side DC link voltage U_{DC2} to 490 V despite the voltage variations on the generator side DC link. The inverter input voltage U_{DC2} regulation is obtained by changing the shoot-through duty cycle Ds [8].

The peak value of the inverter side DC link voltage U_{DC2} is so high due to lower modulation index M if compared with voltage source inverters. Modulation index is limited by shoot-through states implemented in SL qZSI.

The variation range of the voltage conversion ratio G (69) lies between 1.44 and 2.4 that corresponds to the generator side DC link voltage U_{DC1} range from 250 V up to 150 V. Since the modulation index M and the boost factor B are the functions of D_S, the appropriate values of shoot-through can be found for minimum and maximum G values. The variation range of the shoot-through duty cycle D_S is from 0.17 in maximum speed conditions to 0.27 in the cut-in speed conditions.

3.2. Analysis of simulation and experimental results

A series of simulations and experiments were performed to verify the proper operation of the proposed SL qZSI based back-to-back converter. Tests were performed at three characteristic operation points of the VSWT system to demonstrate the converters operation modes in the entire generator voltage and power range [8]. These points are: cut-in speed (low voltage and minimum power), rated speed (corresponds to 7.5 m/s wind speed) and maximum generator speed, power conditions. General parameters of experimental setup based on 1.3 kW PMSG and proposed interface converter are summarized in Table 3.1. The simple boost control technique [8] was implemented for the SL qZSI during simulations and tests. The operating frequency of the SL qZSI network was 10 kHz and maximal switching frequency of transistors – 20 kHz.

Table 3.1

General specifications of experimental setup

Component	Value or type
PMSG	
Phase resistance	1 Ω
Phase inductance	5 mH
Interface converter	
$T_1 \ldots T_6$	600 V/48 A IGBT (IXSH24N60AU1)
$T_{11} \ldots T_{14}$	600 V/12 A IGBT (G4PC30UD)
$D_1 \ldots D_4$	600 V/120 A fast diode (STTH200L06TV)
Capacitance of C	470 uF
Inductance of $L_1 \ldots L_3$	1.2 mH
Capacitance of $C_1 \ldots C_2$	180 uF
Inductance of L_f	100 uH
Capacitance of C_f	2 uF

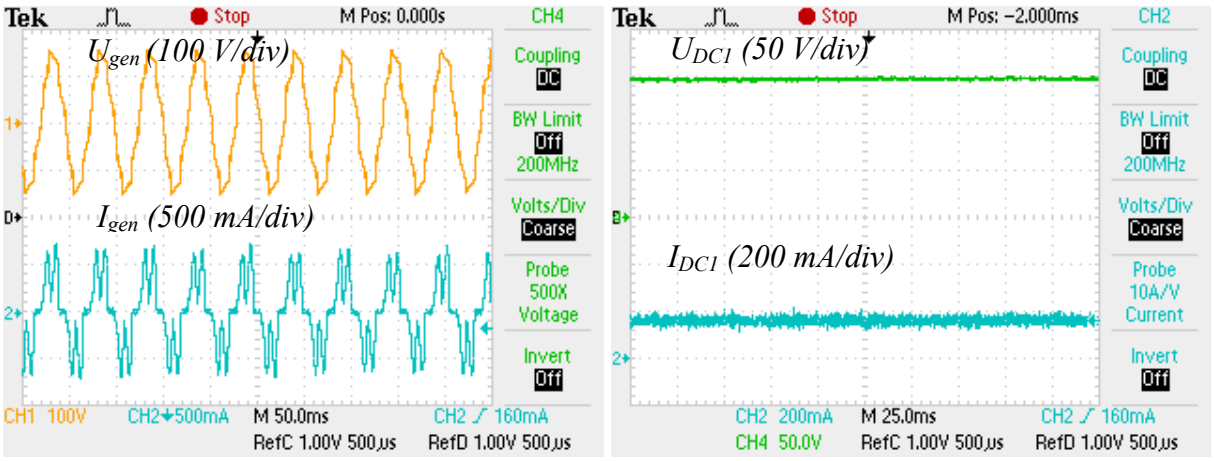
The tests were performed in two stages. First, the operation of PWM rectifier was studied, which is followed by the validation of the SL qZSI.

3.2.1. Analysis of experimental results of PWM rectifier

Experiments with PWM rectifier were performed in order to ensure that there is no need for additional inductors between PMSG and rectifier for proper boost functionality. First test was performed at generator voltage U_{gen} = 53 V and 40 W load, which corresponds to the cut-in speed conditions. Simple boost control was realized by controlling only three lower transistors with the fixed duty cycle at 10 kHz switching frequency. Generator current I_{gen} (Fig. 3.5.*a*) is not sinusoidal due to simple boost control, but the amplitude of the generator voltage U_{gen} appears as 150 V, since this is modulated signal with amplitude equal to DC link voltage U_{DC1} (Fig. 3.5.*b*).

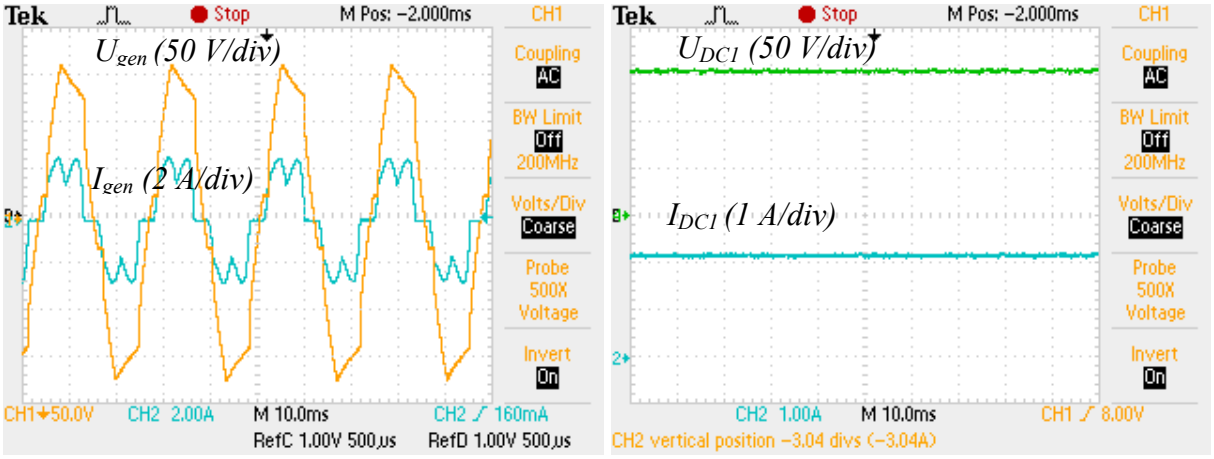
Second test was performed at rated speed conditions, when generator speed is 315 rpm and its power reaches 330 W. The amplitude value of generator voltage U_{gen} reaches 150 V and there is no need for the boost (Fig. 3.6.).

Third test was performed at maximal speed and power of the PMSG: 510 rpm and 1250 W, respectively (Fig. 3.7.). Since the nominal speed of generator is 375 rpm, the test was necessary to verify the generator ability to produce required power at this speed. The amplitude value of generator output voltage reaches 250 V at this point and is maximal input voltage for the SL qZSI.



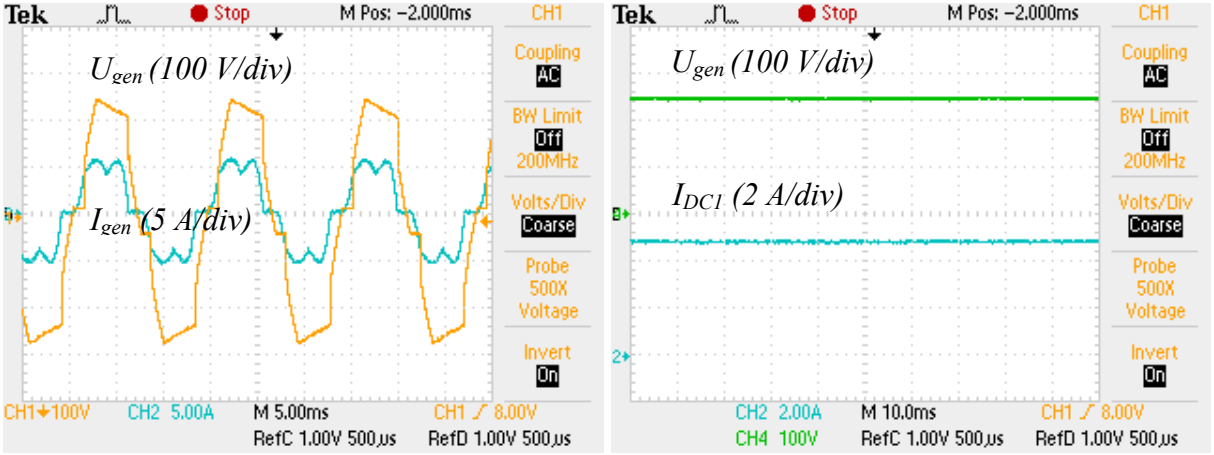
(a) (b)

Fig. 3.5. PMSG voltage and current (a) and generator side DC link voltage and current at 40W



(a) (b)

Fig. 3.6. PMSG voltage and current (a) and generator side DC link voltage and current at 330 W



(a) (b)

Fig. 3.7. PMSG voltage and current (a) and generator side DC link voltage and current (b) at 1250 W

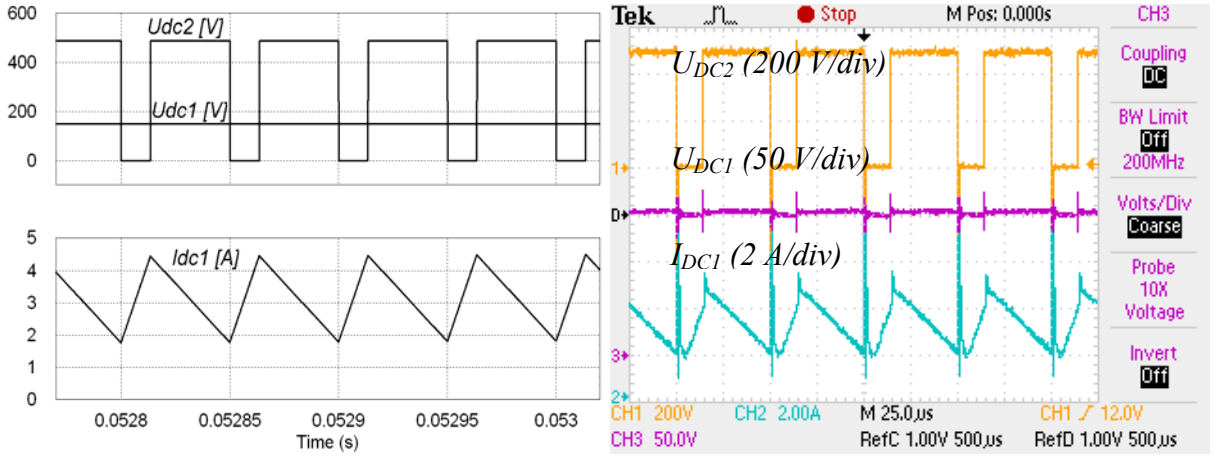
After the experiments it was concluded that the PWM rectifier operates as expected thus ensuring the demanded voltage on the generator side DC link within the whole operation voltage range of the selected PMSG

3.2.2. Analysis of simulation and experimental results of the SL qZSI

First simulations and tests were performed at the generator side DC link voltage of 150 V. The power rating was 330 W. To boost this voltage to the desired level of the intermediate DC link (U_{DC2} = 490 V_{peak}) the shoot-through duty cycle D_S was set to 0.27. Fig. 3.8. shows that the SL qZSI operates in CCM and ensures the demanded gain of the input voltage (U_{DC2} = 490 V_{peak}, as expected).

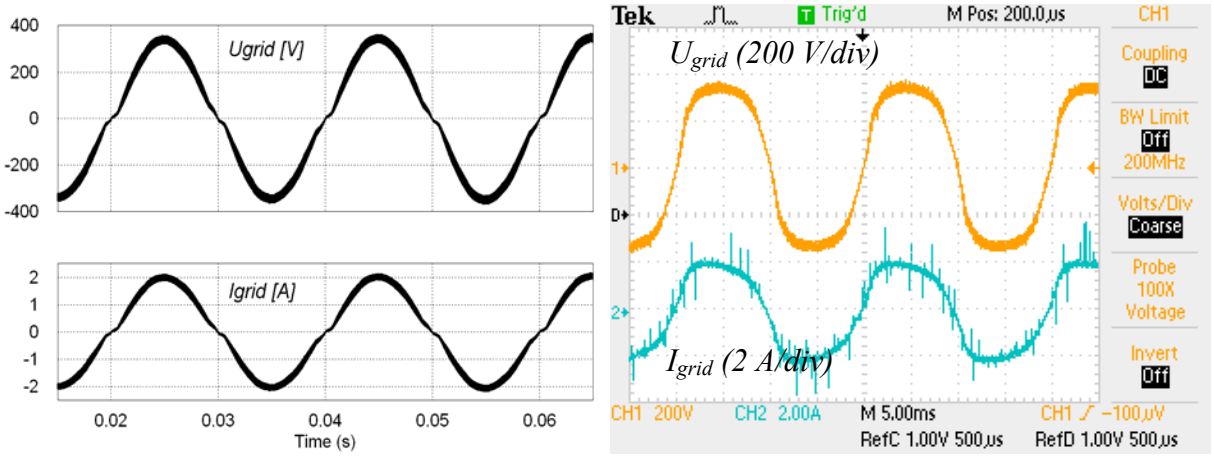
The simulated and experimental waveforms of the grid voltage and current U_{grid} and I_{grid} of the proposed interface converter at this operation point are presented in Fig. 3.9. It is seen that the grid side PWM inverter operates correctly thus ensuring the 230 VAC_{rms} 50 Hz grid voltage.

The second group of simulations and experiments was performed at the generator side DC link voltage of 250 V. The power rating was 1250 W. The shoot-through duty cycle of the SL qZSI was set to 0.17 to ensure necessary voltage boost at this operation point. Both DC link voltages and input current are shown in Fig. 3.10. while the grid voltage and current in Fig. 3.11 Experimental results clearly demonstrate the converter's ability to ensure the required grid voltage level at all operation modes of the interface converter.



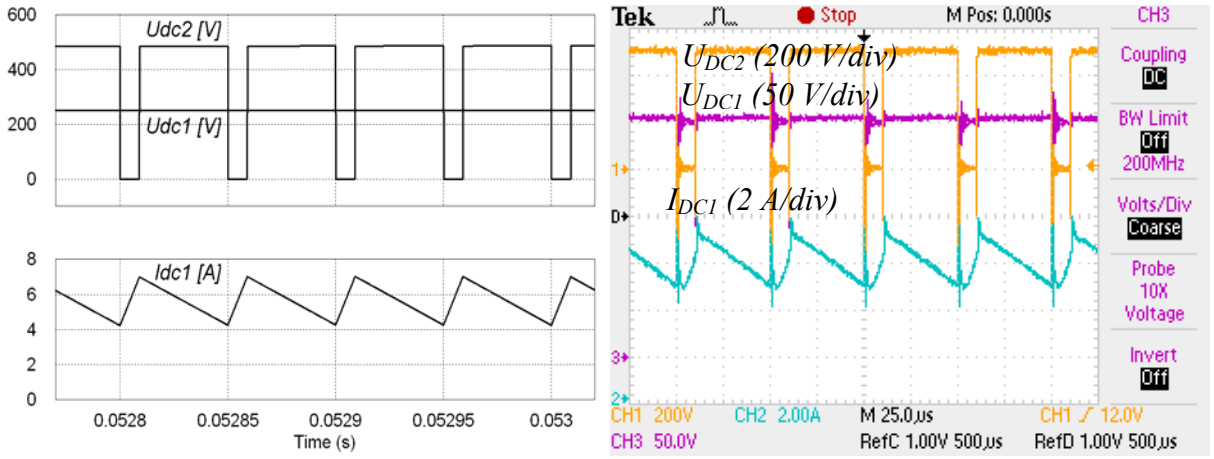
(a) (b)

Fig. 3.8. Simulated (a) and experimental (b) waveforms of operating voltages and input current of the SL qZSI at 330 W



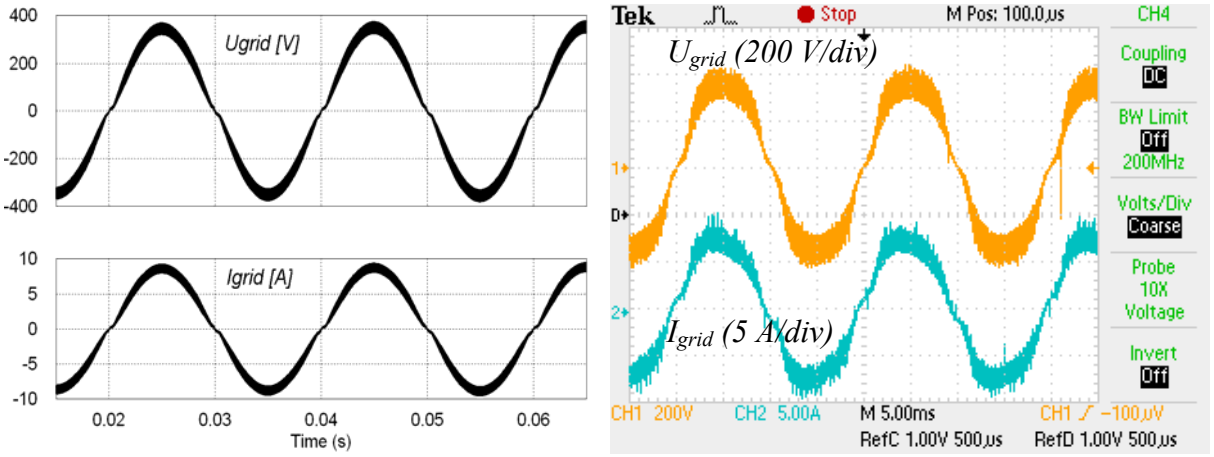
(a) (b)

Fig. 3.9. Simulated (a) and experimental (b) waveforms of the grid voltage and current at 330 W



(a) (b)

Fig. 3.10. Simulated a) and experimental b) waveforms of qZSI voltages and current at 1250W load



(a) (b)

Fig. 3.11. Simulated a) and experimental b) waveforms of SL qZSI output voltage and current at 1250W load

3.3. Power losses of semiconductors in qZS DC/DC converters with HF isolation

Since the direct efficiency measurement of the qZS DC/DC converter with HF isolation can not be made do to absence of calorimeter the power losses in semiconductor switches was evaluated by the simulation software PSIM with thermal module. The model of semiconductor switches was developed according to manufacturer data sheets.

Conduction losses of diode P_{D_con} is calculated by following relation:

$$P_{D\_con} = U_d \cdot I_d , \tag{70}$$

where U_d - is the diode voltage drop;

I_d - is diode forward current.

The diode turn on loses are neglected, but the turn off losses of diode P_{D_sw} is calculated as follows:

$$P_{D\_sw} = \frac{1}{4} Q_{rr} \cdot U_r \cdot f , \tag{71}$$

where Q_{rr} - is reverse recovery charge;

U_r - is reverse blocking voltage;

f - frequency.

Conduction loses of transistor P_{Q_con} is calculated as:

$$P_{Q\_con} = U_{ce} \cdot I_c , \tag{72}$$

where U_{ce} - is the transistor saturation voltage;

I_c - is the collector current.

The turn-on losses of the transistor is calculated as:

$$P_{Q\_turn-on} = E_{on} \cdot f \cdot \frac{U_{ce}}{U_{ce\_datasheet}} , \tag{73}$$

where E_{on} - is the transistor turn-on energy;

f - is the frequency;

U_{ce} - is the actual collector emitter voltage;

$U_{ce\_datasheet}$ - is the datasheet value.

The turn-off loses of transistor is calculated as follows:

$$P_{Q\_turn-off} = E_{off} \cdot f \cdot \frac{U_{ce}}{U_{ce\_datasheet}} , \tag{74}$$

where E_{off} - is the transistor turn-off energy.

The values of semiconductor (diodes and transistors of qZS and voltage doubler rectifier) power losses of qZS DC/DC converter with HF isolation and SL qZS DC/DC converter in proposed interface converter topologies evaluated by PSIM software are collected in Table 3.2

Table 3.2

Power losses of semiconductor switches at different wind conditions (qZS & VDR)

Conditions	Power P_{DC2}	40 W	40 W	330 W	1250 W
	Voltage U_{DC1}	70 V	150 V	150 V	250 V
	Wind speed	3.5 m/s	3.5 m/s	7.5 m/s	12 m/s
Converter topology		*Loses and efficiency (only semiconductor devices)*			
Rectifier & qZSI		4 W / 90 %		17 W / 95 %	37.8 W / 97 %
Rectifier & SL qZSI		3.9 W / 90.2 %		21.5 W / 93.5 %	44.7 W / 96.4 %
Controlled rectifier & qZSI			2.6 W / 93.5 %	17 W / 95 %	37.8 W / 97 %
Controlled rectifier & SL qZSI			3.3 W / 91.7 %	21.5 W / 93.5 %	44.7 W / 96.4 %

3.4. Conclusions

Proposed SL qSZ DC/DC converter with increased boost properties can be successfully implemented in applications where inverted voltage can be directly supplied to distribution network. Thanks to shorter shoot-through duty cycles the range of modulation index M can be wider and total voltage conversion ratio G – higher. Analysis of the power loses in qZS DC/DC converter with voltage doubler rectifier in proposed interface converter topologies (Table 3.2) shows that utilization of controlled rectifier increases the efficiency of DC/DC converter, but taking into account additional power losses caused by controlled rectifier itself the utilization of this topology is less attractive than topology with uncontrolled rectifier, especially in micro power range.

4. CONCLUSIONS AND FUTURE WORK

The family of qZS based interface converters for PMSG based VSWT applications are offered in this thesis The qZS based interface converter with generator side inverter was offered for PMSG based VSWT systems in small power range, but topology with uncontrolled rectifier for micro power range.

The new topology of qZS converter with switched inductors was offered and analysed. The main target for this topology is converters with ultra wide input voltage range, thanks to enhanced boost performance of this converter. The main advantage of the proposed converter is the enhanced output voltage regulation properties thanks to the new SL qZS network implemented. The proposed topology could be implemented in the residential PMSG based wind turbines with power rating up to 15 kW.

The future work should be concentrated on brand new semiconductor switch utilisation in converters for future efficiency optimization and higher utilization of renewable energy.

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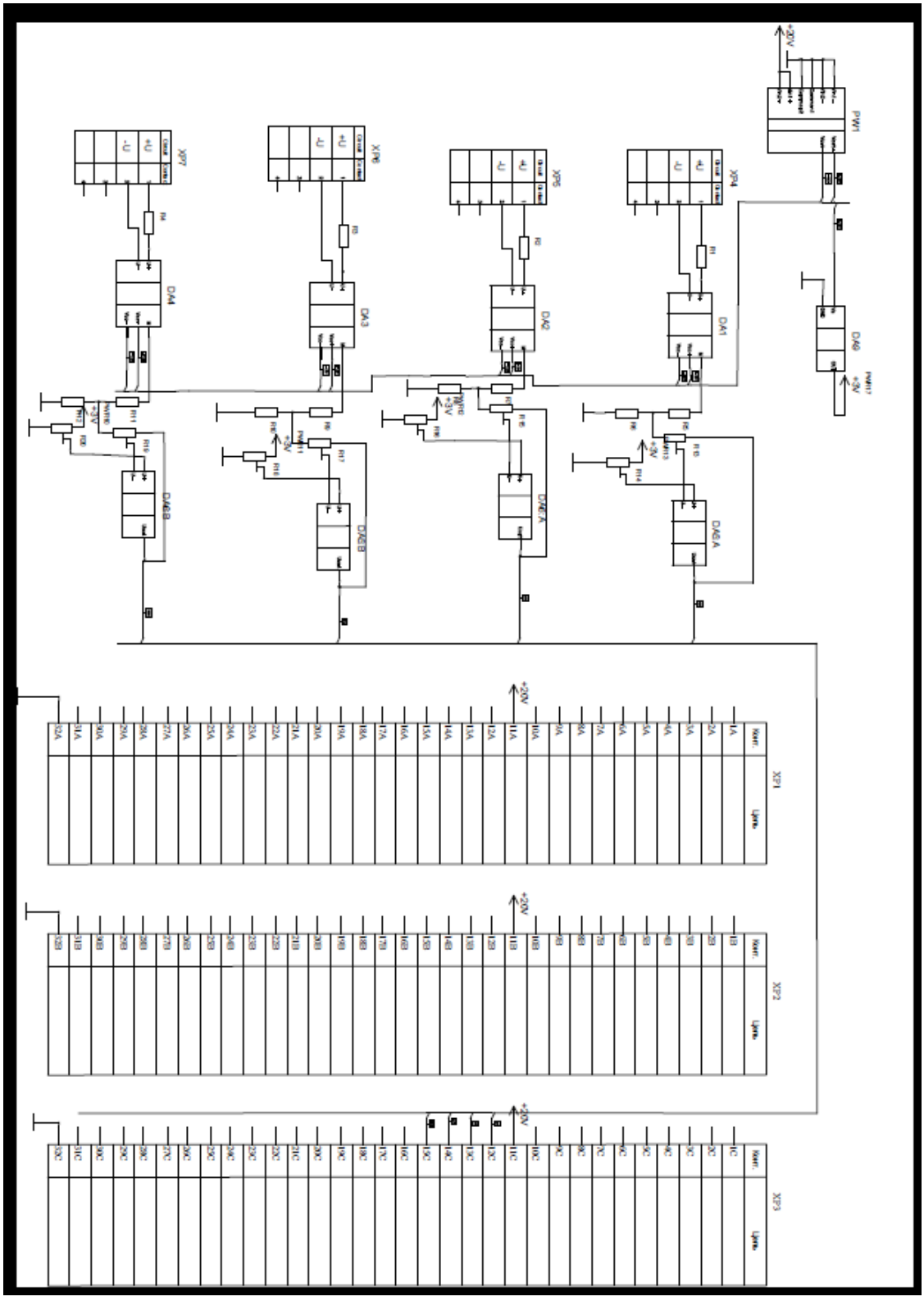
APPENDIXES

1. VOLTAGE MEASUREMENT



2. C-code of controlled rectifier control

```
#include "DSP2833x_Examples.h"   // DSP2833x Examples Include File
```

```
#include <math.h>
#include <stdio.h>
#include <file.h>
#include <stdlib.h>
#include <limits.h>

// LOCAL ABBREVIATIONS AND CONSTANTS
//-----------------------------------------------------------------------------------------------------------
#define EPWM1_PRD 1995
#define Udc_ref 18205 //150V
#define Kint 10000000
#define opened 900
#define closed 0
#define PI 3.141592654

// LOCAL FUNCTION PROTOTYPES
//-----------------------------------------------------------------------------------------------------------
void Set_Pwm(void);
void Configure_ADC(void);
interrupt void Change_PWM_duty(void);

//-----------------------------------------------------------------------------------------------------------
// FUNCTIONS
//-----------------------------------------------------------------------------------------------------------
float Udc, ia, ib, ic, irefa, irefb, irefc, S=0, scale=-0.1;
signed int Ua_int, Ub_int, Uc_int, Udc_int, ia_int, ib_int, ic_int;
float ADC_dc_vector[10];
unsigned int ADC_res[7];
float ADC_sum;

void main(void)
{
   InitSysCtrl(); // general clock settings
 EALLOW;
```

```
  #if (CPU_FRQ_150MHZ)            // Default - 150 MHz SYSCLKOUT

        #define ADC_MODCLK 0x3 // HSPCLK = SYSCLKOUT/2*ADC_MODCLK2 =
150/(2*3)         = 25.0 MHz
  #endif
  #if (CPU_FRQ_100MHZ)

        #define ADC_MODCLK 0x2 // HSPCLK = SYSCLKOUT/2*ADC_MODCLK2 =
100/(2*2)         = 25.0 MHz
  #endif

  EDIS;
        InitEPwm1Gpio(); //initialization of PWM signal
        InitEPwm2Gpio();
        InitEPwm3Gpio();
   InitEPwm4Gpio();
        InitEPwm5Gpio();
        InitEPwm6Gpio();
   DINT;

   InitPieCtrl();
        InitAdc();  // initialization of AD converter
        InitEPwm();
        Configure_ADC(); // set common configuration of AD converter
        Set_Pwm(); // set settings configuration of PWM
        EPwm1Regs.ETCLR.bit.INT = 1;
        IER = 0xFFFF; //
        IFR = 0x0000; //
   InitPieVectTable(); // settings of Interrupt vector table

   EALLOW;  // This is needed to write to EALLOW protected registers
   PieVectTable.EPWM1_INT = &Change_PWM_duty;
   EDIS;    // This is needed to disable write to EALLOW protected registers
   EALLOW;
```

```
    SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0;
    EDIS;

    EALLOW;
    SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;
    EDIS;

    IER |= M_INT3;  // Enable group 3 CPU interrupts
    PieCtrlRegs.PIEIER3.bit.INTx1 = 1;         // Enable interrupt 1 in group 3

    EINT;   // Enable Global interrupt INTM
    ERTM;   // Enable Global realtime interrupt DBGM

    for(;;)
    {
      asm("NOP");
    }
}
```

```
/*************************************************************************
*   @brief Initializing of timers 1, 2, 3
*/
/*************************************************************************
/
void Set_Pwm()
{
        EPwm1Regs.TBPRD                         = EPWM1_PRD;            //
Set timer 1 period
        EPwm2Regs.TBPRD                         = EPWM1_PRD;            //
Set timer 2 period
        EPwm3Regs.TBPRD                         = EPWM1_PRD;            //
Set timer 3 period


        EPwm1Regs.TBPHS.half.TBPHS      = 0x0000;               // Set timer
1 phase 0
        EPwm2Regs.TBPHS.half.TBPHS      = 0x0000;               // Set timer
2 phase 0
        EPwm3Regs.TBPHS.half.TBPHS      = 0x0000;               // Set timer
3 phase 0

        EPwm1Regs.TBCTR                         = 0x0000;               //
Clear counter
        EPwm2Regs.TBCTR                         = 0x0000;               //
Clear counter
        EPwm3Regs.TBCTR                         = 0x0000;               //
Clear counter
```

```
// Initializing compare registers
//-----------------------------------------------------------------------------------------------
EPwm1Regs.CMPA.half.CMPA        = 0;
EPwm2Regs.CMPA.half.CMPA        = 0;
EPwm3Regs.CMPA.half.CMPA        = 0;
EPwm1Regs.CMPB          = 0;
EPwm2Regs.CMPB          = 0;
EPwm3Regs.CMPB          = 0;
//-----------------------------------------------------------------------------------------------
// Action when the counter equals the active CMPA register and the counter is incrementing
// 0x0000 (00) Do nothing (action disabled)
// 0x0001 (01) Clear: force EPWM1A/EPWM1B output low
// 0x0002 (10) Set: force EPWM1A/EPWM1B output high
// 0x0003 (11) Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low
//-----------------------------------------------------------------------------------------------
EPwm1Regs.AQCTLA.bit.CAU        = 0x0001;
EPwm2Regs.AQCTLA.bit.CAU        = 0x0001;
EPwm3Regs.AQCTLA.bit.CAU        = 0x0001;
EPwm1Regs.AQCTLB.bit.CBU        = 0x0001;
EPwm2Regs.AQCTLB.bit.CBU        = 0x0001;
EPwm3Regs.AQCTLB.bit.CBU        = 0x0001;
//-----------------------------------------------------------------------------------------------
// Action when the counter equals the active CMPA register and the counter is decrementing
// 0x0000 (00) Do nothing (action disabled)
// 0x0001 (01) Clear: force EPWMxA output low
// 0x0002 (10) Set: force EPWMxA output high
// 0x0003 (11) Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low
//-----------------------------------------------------------------------------------------------
EPwm1Regs.AQCTLA.bit.ZRO        = 0x0002;
EPwm2Regs.AQCTLA.bit.ZRO        = 0x0002;
```

```
        EPwm3Regs.AQCTLA.bit.ZRO            = 0x0002;
        EPwm1Regs.AQCTLB.bit.ZRO            = 0x0002;
        EPwm2Regs.AQCTLB.bit.ZRO            = 0x0002;
        EPwm3Regs.AQCTLB.bit.ZRO            = 0x0002;
        return;
}



interrupt void Change_PWM_duty(void)
{

unsigned int tmp1;

                if(AdcRegs.ADCST.bit.SEQ1_BSY==0)
        {
                ADC_res[0] = (AdcRegs.ADCRESULT1 ); //Ua
                ADC_res[1] = (AdcRegs.ADCRESULT3 ); //Ub
                ADC_res[2] = (AdcRegs.ADCRESULT5 ); //Uc
                ADC_res[3] = (AdcRegs.ADCRESULT7 ); //Udc
                ADC_res[4] = (AdcRegs.ADCRESULT9 ); //Ia
                ADC_res[5] = (AdcRegs.ADCRESULT11);//Ib
                ADC_res[6] = (AdcRegs.ADCRESULT13);//Ic
                }

AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;               // Reset SEQ1 set CONV to 0
                AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;
```

```
//----------------------------Keskmiste arvutamine--------------------

Ua_int = ADC_res[0]-32768;
Ub_int = ADC_res[1]-32768;
Uc_int = ADC_res[2]-32768;
Udc_int= ADC_res[3]-31768;
ia_int = ADC_res[4]-32768;
ib_int = ADC_res[5]-32768;
ic_int = ADC_res[6]-32768;
Udc_int=Udc_int*(-1);

        for (tmp1=1; tmp1<=9; tmp1++)
        {
        ADC_dc_vector[tmp1]=ADC_dc_vector[tmp1-1];
        }

        ADC_dc_vector[0] = Udc_int;
        ADC_sum=0;
        for (tmp1=0; tmp1<=9; tmp1++)

        {
        ADC_sum=ADC_sum+ADC_dc_vector[tmp1];
        }

        Udc=ADC_sum/10;



S = S+(Udc_ref-Udc)/Kint;
if (S>2) {S=2;} else {};
irefa=S*scale*Ua_int;
irefb=S*scale*Ub_int;
irefc=S*scale*Uc_int;
ia=-1*scale*ia_int;
```

```
ib=-1*scale*ib_int;
ic=-1*scale*ic_int;


if (irefa>=0 && ia<=irefa)

{       EPwm1Regs.CMPA.half.CMPA = opened;
        EPwm1Regs.CMPB = opened;
}

else
        if (irefa<=0 && ia>=irefa)

        {       EPwm1Regs.CMPA.half.CMPA = closed;
                EPwm1Regs.CMPB = opened;
        }

        else

        {       EPwm1Regs.CMPA.half.CMPA = closed;
                EPwm1Regs.CMPB = closed;}


                if (irefb>=0 && ib<=irefb)

{       EPwm2Regs.CMPA.half.CMPA = opened;
        EPwm2Regs.CMPB = opened;
}

else
        if (irefb<=0 && ib>=irefb)

        {       EPwm2Regs.CMPA.half.CMPA = closed;
                EPwm2Regs.CMPB = opened;
```

```
        }
        else

        {       EPwm2Regs.CMPA.half.CMPA = closed;
                EPwm2Regs.CMPB = closed;}

                if (irefc>=0 && ic<=irefc)

{       EPwm3Regs.CMPA.half.CMPA = opened;
        EPwm3Regs.CMPB = opened;
}

else
        if (irefc<=0 && ic>=irefc)

        {       EPwm3Regs.CMPA.half.CMPA = closed;
                EPwm3Regs.CMPB = opened;
        }

        else

        {       EPwm3Regs.CMPA.half.CMPA = closed;
                EPwm3Regs.CMPB = closed;}
 // Clear INT flag for this timer
    EPwm1Regs.ETCLR.bit.INT = 1;
  // Acknowledge this interrupt to receive more interrupts from group 3
  PieCtrlRegs.PIEACK.all = PIEACK_GROUP3;

return;

}

void Configure_ADC(void)
```

```
{
    AdcRegs.ADCTRL1.bit.SEQ_CASC = 1;        // cascaded seqence mode 1
    AdcRegs.ADCTRL3.bit.SMODE_SEL = 1;       //simultanious mode of
conversations
    AdcRegs.ADCTRL1.bit.CONT_RUN = 0;        //Start stop mode. Stop after each
sequence
    AdcRegs.ADCMAXCONV.all = 0x000F;         // Autoconvertion mode, 16
conv's on SEQ

    AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x00;  // Setup Pin Ua as 1st SEQ1 conv.
    AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 0x01;  // Setup Pinge Ub
    AdcRegs.ADCCHSELSEQ1.bit.CONV02 = 0x02;  // Setup for Uc
    AdcRegs.ADCCHSELSEQ1.bit.CONV03 = 0x03;   // Setup for Udc
    AdcRegs.ADCCHSELSEQ2.bit.CONV04 = 0x04;   // Setup for Ia
    AdcRegs.ADCCHSELSEQ2.bit.CONV05 = 0x05;  // Setup Pinge Ib
    AdcRegs.ADCCHSELSEQ2.bit.CONV06 = 0x06;  // Setup for Ic
    AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x9;   // Setup Pinge Ua as 1st SEQ1
conv.
    AdcRegs.ADCCHSELSEQ2.bit.CONV07 = 0x07;
    AdcRegs.ADCCHSELSEQ3.bit.CONV08 = 0x08;   // Setup for Ia
    AdcRegs.ADCCHSELSEQ3.bit.CONV09 = 0x09;  // Setup Pinge Ib
    AdcRegs.ADCCHSELSEQ3.bit.CONV10 = 0x0A;  // Setup for Ic
    AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x9;   // Setup Pinge Ua as 1st SEQ1
conv.
    AdcRegs.ADCCHSELSEQ3.bit.CONV11 = 0x0B;
    AdcRegs.ADCCHSELSEQ4.bit.CONV12 = 0x0C;   // Setup for Ia
    AdcRegs.ADCCHSELSEQ4.bit.CONV13 = 0x0D;  // Setup Pinge Ib
    AdcRegs.ADCCHSELSEQ4.bit.CONV14 = 0x0E;  // Setup for Ic
    AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x9;   // Setup Pinge Ua as 1st SEQ1
conv.
    AdcRegs.ADCCHSELSEQ4.bit.CONV15 = 0x0F;

    AdcRegs.ADCTRL2.bit.EPWM_SOCA_SEQ1 = 1;// Enable SOCA from ePWMA to
start SEQ1
```

```
        AdcRegs.ADCTRL2.bit.INT_ENA_SEQ1 = 0;       // Disable SEQ1 interrupt (every
EOS)
        AdcRegs.ADCREFSEL.bit.REF_SEL = 0;          // sisene ref pingeallikas
        AdcRegs.ADCTRL1.bit.CPS = 0;                // perapheral clock divider
        AdcRegs.ADCTRL3.bit.ADCCLKPS = 3;           // adc clock prescaler
return;
}
```