Simulation Study of High Step-Up Quasi-Z-Source DC-DC Converter with Synchronous Rectification

Liisa Liivik (*PhD Student, Tallinn University of Technology*),
Dmitri Vinnikov (*Principal Research Fellow, Tallinn University of Technology/Riga Technical University*),
Janis Zakis (*Senior Research Fellow, Riga Technical University*)

***Abstract* – This paper discusses the performance improvement method of the recently popular galvanically isolated quasi-Z-source DC-DC converter. In order to decrease the conduction losses in the quasi-Z-source network and voltage doubler rectifier the replacement of diodes by the N-channel MOSFETs was analyzed. The proposed approach was validated by the computer simulations in PSIM environment with accurate models of the semiconductors based on the device datasheet values. Finally, the power losses and resulting efficiency of the proposed quasi-Z-source DC-DC converter with synchronous rectification were compared to those of the traditional topology.**

***Keywords* – DC-DC power converters, Energy efficiency, Pulse width modulation converters.**

I. Introduction

Quasi-Z-Source DC-DC (qZS DC-DC) converter is a new emerged topology from the step-up DC-DC converter family. It could be realized either as the transformerless or the galvanically isolated converter. In the first case the topology is quite similar to the traditional boost converter and can be used as the maximum power point tracker (MPPT) for the photovoltaic (PV) applications [1]. The converter demonstrates high efficiency even at the threefold input voltage gain therefore could be used as the front-end voltage preregulator in the fuel cell power systems of other similar applications with the varying input voltage. The galvanically isolated qZS DC-DC converter has the intermediate AC link with the high frequency transformer [2], which allows setting the desired input voltage gain simply by changing the turns ratio of the transformer. In high gain applications the transformer also plays the role of a galvanic isolation, required in several cases. Furthermore, in the PV power systems the galvanic isolation is essential to reduce ground leakage currents and grid current total harmonic distortion [3].

In [4] the practical realization challenges of the qZS DC-DC converter with galvanic isolation are reported. From one side the topology features such benefits as continuous input current, low start up inrush current, converterless integration of short-term energy storages, soft switching of transistors during active states and the inherent "shoot-circuit immunity" caused by the properties of the qZS-network. From another side, the converter suffers from the lack of efficiency at the high shoot-through duty cycle values, which is mostly caused by the increased power dissipation in the qZS diode *D* (Fig. 1*a*) [5]. The implementation of module integrated freewheeling diodes as rectifiers described in [6] could also decrease the efficiency and affect the performance of the qZS DC-DC converter, especially in the applications with bidirectional power flow.

This paper discusses the performance improvement method of the recently popular galvanically isolated qZS DC-DC converter by the replacement of all the diodes by the controlled switches (preferably, MOSFETs). The design issues, control principles and analysis of the resulting efficiency rise are reported.

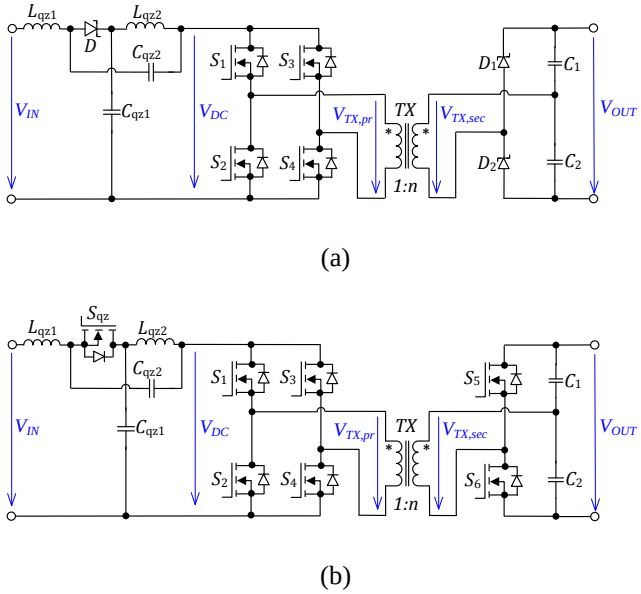

Fig. 1. qZS DC-DC converters with galvanic isolation: traditional (a) and proposed approach, where the diodes are replaced by the N-channel MOSFETs (b).

II. Design and Control Issues

As it was stated before, the diode *D* is one of the main sources of power dissipation in the traditional qZS DC-DC converter (Fig. 1*a*). This diode is reverse biased during the shoot-through states (Fig. 2*a*) and starts conduction during the active states of the converter (Figs. 2*b* and 2*c*). In the conditions of varying input voltage V_{IN} the output voltage of the qZS DC-DC converter V_{OUT} could be regulated by the variation of the shoot-through duty cycle D_S:

$$V_{OUT} = 2 \cdot V_{IN} \cdot n \cdot \left(\frac{1}{1 - 2 \cdot D_S} \right), \qquad (1)$$

where n is the turns ratio of the isolation transformer ($n=V_{TX,sec}/V_{TX,pr}$).

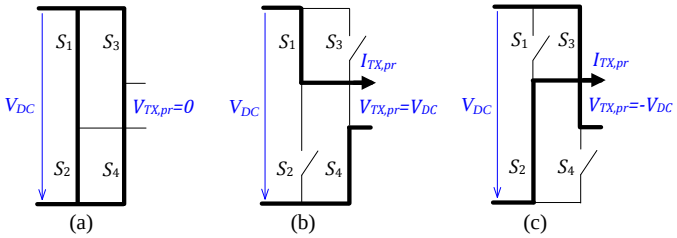

Fig. 2. Main operating states of the front-end inverter: shoot-through (a) and active states (b and c).

The simplest and most efficient method of the shoot-through states generation is the overlap of the active states, shown in Fig. 3 [7]. The duty cycle of active states of transistors is greater than or equal to 0.5. If the duty cycle of active states is greater than 0.5 the cross-conduction of top and bottom transistors (shoot-through) will occur in both inverter legs. During this operating mode the current through inverter switches reaches its maximum, the transformer voltage ($V_{TX,pr}$) drops to zero. From the practical point of view due to the conduction losses in semiconductors it is not advisable to operate at the shoot-through duty cycles higher than 0.33. Basically, the diode D of the qZS-network is only needed to avoid short-circuiting of the capacitors C_{qz1} and C_{qz2} during the shoot-through states. At the same time the diode will noticeably increase conduction losses during the active states. To minimize those losses, the N-channel MOSFET S_{qz} could be placed instead the diode D, as shown in Fig. 1*b*. The basic idea and main challenges of such modification were explained in [8]. In the given application the S_{qz} is synchronized with the inverter switches and it only conducts during the active state and blocks the current during the shoot-through (Table I).

TABLE I

SWITCHING STATES SEQUENCE PER ONE PERIOD (FRONT-END INVERTER AND SYNCHRONOUS QZS-NETWORK)

	Top side		**Bottom side**		**Synchr. switch**
	S_1	S_3	S_2	S_4	S_{qz}
Active state	x			x	x
Shoot-through	x	X	x	x	
Active state		X	x		x
Shoot-through	x	X	x	x	

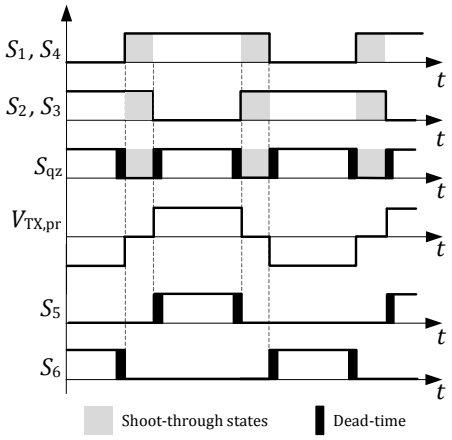

Fig. 3. Proposed control principle of the qZS DC-DC converter with synchronous rectification.

To prevent damage of the circuit, it is advisable to add small dead-time (100 ns…400 ns, depending on the application) before the turn on and off transients of the S_{qz}, as shown in Fig. 3. From the opposite side, it is not recommended to have a dead-time longer than 1 us in order to limit the conduction time of the body diode, and, therefore, to decrease the power losses.

Similarly to qZS-network the conduction losses can be reduced also in the diodes D_1 and D_2 of the voltage doubler rectifier (VDR). Fig. 3 shows the control principle of the synchronized VDR based on the N-channel MOSFETS S_5 and S_6. As it is seen from the diagram the dead-time is also necessary before the turn on and off transients of the S_5 and S_6.

III. COMPARATIVE ANALYSIS OF POWER LOSSES AND EFFICIENCY

To estimate the efficiency rise available from the proposed approach, the power loss analysis was performed in the PSIM simulation environment by using the Thermal Module. In this software the switching and conduction losses of the semiconductor are calculated based on the device datasheet values. For the primary side of the converter the dual trench MOS barrier Shottky rectifier Vishay V60D100C with externally paralleled diodes was compared to synchronous switch realized on an N-channel MOSFET Vishay Si4190ADY. For the secondary side the SiC Shottky rectifiers CREE C3D02060E were compared to the synchronized VDR based on the SiC MOSFETs ROHM SCT2120AF. The generalized specifications of semiconductors are presented in Table II and the simulation parameters of the circuit were set according to the data presented in Table III.

TABLE II

SEMICONDUCTOR COMPONENTS SELECTED FOR THE POWER LOSS ANALYSIS

Component	Type	Specifications
$S_1…S_4$, S_{qz}	Vishay Si4190ADY	V_{DS}=100 V; $R_{DS(on)}$=8.8 mΩ I_D=18.4 A, Q_g=20.7 nC, R_g=2.2 Ω
D	Vishay V60D100C	V_{RRM}=100 V; V_F=0.66 V $I_{F(AV)}$=2x30 A (common cathode)
D_1, D_2	CREE C3D02060E	V_{RRM}=600 V; V_F=1.8 V $I_{F(AV)}$=4 A
S_5, S_6	ROHM SCT2120AF	V_{DS}=650 V; $R_{DS(on)}$=120 mΩ I_D=29 A, Q_g=61 nC, R_g=2.5 Ω

TABLE III

SIMULATION PARAMETERS OF THE HIGH STEP-UP QZS DC-DC CONVERTER

Parameter	Symbol	Value
Input voltage range, V	V_{IN}	15…30
Maximum input current, A	I_{IN}	10
Peak DC-link voltage, V	$V_{DC(peak)}$	30
Output voltage, V	V_{OUT}	300
Switching frequency, kHz	f_{sw}	100
Operating frequency of qZS-network, kHz	f_{qZS}	200 ($2 \cdot f_{sw}$)
Transformer turns ratio	n	5

Capacitance of qZS capacitors, uF	C_{qz1}, C_{qz2}	26.4
Inductance of qZS inductors, µH	L_{qz1}, L_{qz2}	22
Capacitance of output capacitors, uF	C_1, C_2	2.2
Converter power rating, W	P	300

The power losses and efficiency were estimated in four test points with operating conditions described in Table IV. The load resistor R_L was adjusted to achieve the maximum input current in every operating point.

TABLE IV

SHOOT-THROUGH DUTY CYCLE, RESISTANCE OF THE LOAD AND OPERATING POWER IN THE SELECTED TEST POINTS

Test point	1	2	3	4
V_{IN}, V	15	20	25	30
D_S	0.25	0.167	0.083	0
R_L, Ω	600	450	360	300
P, W	150	200	250	300

IV. ANALYSIS OF SIMULATION RESULTS

First, the possible benefits of the synchronous rectification (SR) in the qZS-network were studied. The compared converters had fully identical inverter stages, isolation transformers and VDRs, the difference lied only in the realization of the qZS-networks (diode vs. MOSFET). Fig. 4 shows the comparison of conduction and switching losses of both designs within the studied operating range of the converter. The Shottky diode implemented in the traditional qZS-network features almost zero switching losses, however, its conduction losses are more than twice higher than those of MOSFET in the synchronized qZS-network. Finally, it resulted in more than 1.2% efficiency rise within the whole operating range of the studied DC-DC converter (Fig. 5). The efficiency could be further increased by the implementation of eGaN FETs with ultra-low RDS(ON) (up to 3.2 mΩ, [9]).

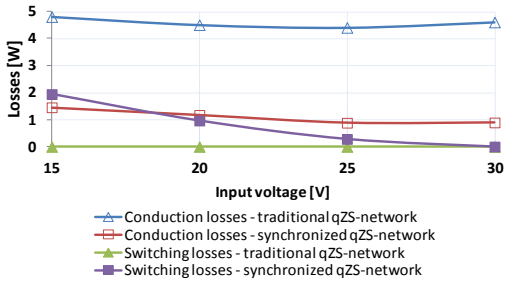

Fig. 4. Semiconductor power losses of the traditional and synchronized qZS-networks in the studied operating range of the converter.

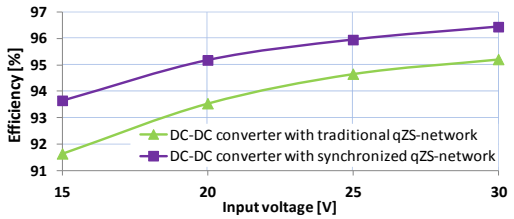

Fig. 5. Efficiency comparison of the qZS DC-DC converter with traditional and synchronized qZS-networks.

In our case study the 200 ns dead-time was implemented before the turn on and off transients of the synchronous switch S_{qz}. Taking into account that the qZS-network operates with twice switching frequency of the converter the selected dead-time formed 4 % of the operating period of the synchronous switch. In order to understand the influence of the dead-time on the efficiency of the DC-DC converter a series of simulations was performed. The dead-time was changed with the variable steps from 200 ns to 2 us. It is seen from Fig. 6 that threefold increase of the dead-time will result in almost 1% of the efficiency drop at the minimum input voltage, when the shoot-through duty cycle reaches its maximum. If the dead-time will be increased to 2 us the benefits of SR will be almost cancelled since the resulting efficiency will be quite close to that of the DC-DC converter with traditional qZS-network.

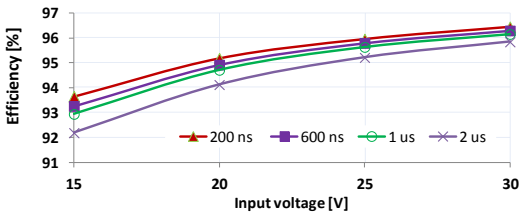

Fig. 6. Influence of the dead-time on the efficiency of the qZS DC-DC converter with synchronized qZS-network.

Next, the possible benefits of the SR in the VDR were analyzed. The compared converters had fully identical inverter stages and diode based qZS-network explained before but this time the difference lied in the realization of the VDR (diode vs. MOSFET). Fig. 7 shows the comparison of conduction and switching losses of both discussed designs within the studied operating range of the converter. Typically, application of the VDR in the galvanically isolated DC-DC converters is associated with the soft switching of semiconductors used in it, therefore, both approaches demonstrate near zero switching losses.

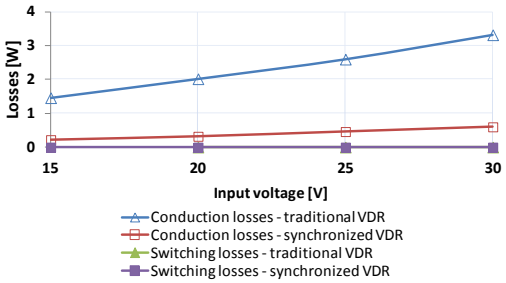

Fig. 7. Semiconductor power losses of the traditional and synchronized VDR in the studied operating range of the converter.

In the studied VDR, conduction losses of the N-channel SiC MOSFET operated with 200 ns dead-time were more than 5 times smaller than those of SiC diode, which resulted in about 1 % higher efficiency of the topology with synchronized VDR.

Finally, it was found that the implementation of SR in the high step-up qZS DC-DC converter could provide the overall efficiency improvement of the converter from 2 % to 3 %, depending on the operation point (Fig. 9).

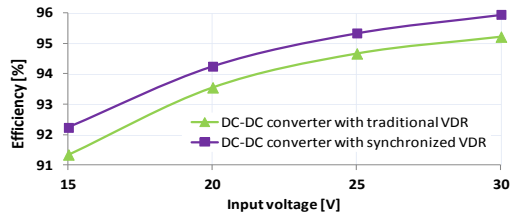

Fig. 8. Efficiency comparison of the qZS DC-DC converter with traditional and synchronized VDRs.

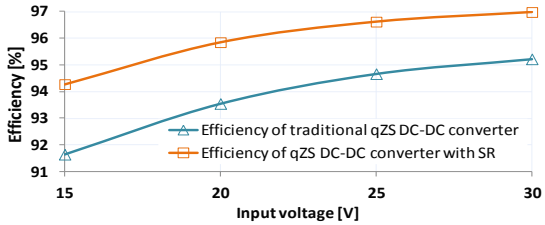

Fig. 9. Overall efficiency rise of the step-up qZS DC-DC converter resulted by the implementation of the synchronized qZS-network and VDR.

V. Conclusions

In this paper the benefits of synchronous rectification in the high step-up qZS DC-DC converter were analyzed. It was shown that due to decreased conduction losses the replacement of diodes by the N-channel MOSFETS in the qZS-network and voltage doubler rectifier could result in the efficiency rise by more than 2 % within the whole operation range of the converter. In order to maximize the efficiency, special attention should be paid to the proper selection of the dead-time before the turn on and off transients of the the synchronous switches to limit the conduction of body diode.

Recent efforts of the research group are directed toward the development of the experimental setup of the step-up qZS DC-DC converter with synchronous rectification. This test bench will be used for validation of the proposed ideas as well as for the study of implementation possibilities of GaN MOSFETs for further efficiency improvement of the converter.

Acknowledgements

This research work was co-financed by Estonian Ministry of Education and Research (project SF0140016s11), Estonian Research Council (Grant G8538) and European Social Fund. Latvian partner research work has been supported by Latvian Council of Science (Grant 416/2012).

References

[1] Zakis, J., Rankis, I., Ribickis, L., "Comparative analysis of boost and quasi-Z-Source Converters as Maximum Power Point Trackers for PV panel integrated converters," IEEE 23rd International Symposium on Industrial Electronics (ISIE), 2014, pp.1991,1995, 1–4 June 2014.

[2] Vinnikov, D., Roasto, I, "Quasi-Z-Source-Based Isolated DC/DC Converters for Distributed Power Generation," IEEE Transactions on Industrial Electronics, vol.58, no.1, pp.192,201, Jan. 2011.

[3] LaBella, T., Lai, J.S., "A Hybrid Resonant Converter Utilizing a Bidirectional GaN AC Switch for High-Efficiency PV Applications," Twenty-Ninth Annual IEEE Applied Power Electronics Conference and Exposition, 2014. pp.1,8, 16-20 Mar. 2014.

[4] Vinnikov, D., Roasto, I., Zakis, J., Strzelecki, R. "New Step-Up DC/DC Converter for Fuel Cell Powered Distributed Generation Systems: Some Design Guidelines". Przeglad Elektrotechniczny, vol. 86 (8), pp. 245–252, 2010.

[5] Vinnikov, D.; Roasto, I, "Impact of component losses on the voltage boost properties and efficiency of the qZS-converter family," 7th International Conference-Workshop Compatibility and Power Electronics (CPE), pp. 303,308, 1–3 June 2011.

[6] Vinnikov, D.; Roasto, I; Zakis, J., "New bi-directional DC/DC converter for supercapacitor interfacing in high-power applications," 2010 14th International Power Electronics and Motion Control Conference (EPE/PEMC), pp.T11-38, T11-43, 6–8 Sept. 2010.

[7] Roasto, I., Vinnikov, D., Jalakas, T., Zakis, J., Ott, S., "Experimental study of shoot-through control methods for qZSI-based DC/DC converters," 2010 International Symposium on Power Electronics Electrical Drives Automation and Motion (SPEEDAM), pp. 29,34, 14–16 June 2010.

[8] Liivik, L., Vinnikov, D., Jalakas, T., "Synchronous Rectification in Quasi-Z-Source Converters: Possibilities and Challenges". 2014 IEEE International Conference on Intelligent Energy and Power Systems (IEPS2014), pp 32–35, June 2–6, 2014, Kyiv, Ukraine.

[9] [Online]. Available: http://epc-co.com/epc/Products [Accessed: Aug. 3, 2014].

Liisa Liivik received Dipl.-Eng and M. Sc. in Electrical Engineering from the Department of Electrical Drives and Power Electronics, Tallinn University of Technology, Tallinn, Estonia, in 1998 and 2000, respectively. She is currently working toward the Ph.D. degree at the Department of Electrical Engineering of TUT.

Her fields of interest include research, design and simulation of switch mode converters for distributed power generation systems. She is author or co-author of more than 10 scientific papers and 1 book.

Tallinn University of Technology, Department of Electrical Engineering. Address: Ehitajate tee 5, 19086 Tallinn, Estonia; E-mail: liisa.liivik.ee@ieee.org

Dmitri Vinnikov (M'07 - SM'11) received the Dipl. Eng., M. Sc., and Dr. Sc. techn. degrees in electrical engineering from Tallinn University of Technology, Tallinn, Estonia, in 1999, 2001, and 2005, respectively.

He is currently a Head of the Power Electronics Research Group at the Department of Electrical Engineering, Tallinn University of Technology and Scientific Consultant at the Institute of Industrial Electronics and Electrical Engineering, Riga Technical University. He has authored more than 150 published papers on power converter design and development and is the holder of several Patents and Utility Models in this field.

Tallinn University of Technology, Department of Electrical Engineering. Address: Ehitajate tee 5, 19086 Tallinn, Estonia

E-mail: dmitri.vinnikov@ieee.org.

Janis Zakis (M'10 – SM'14) received B. Sc., M. Sc. and Dr. Sc. ing. in electrical engineering from Riga Technical University, Riga, Latvia, in 2002, 2004 and 2008, respectively.

He is presently a Senior Researcher in the Institute of Industrial Electronics and Electrical Engineering, Riga Technical University.

He has over 20 publications and is the holder of the Utility Model in power converter design. His research interests include flexible ac transmission systems (FACTS), simulation of power systems, switching mode power converters, applied design of power converters and energy storage systems.

Riga Technical University, Institute of Industrial Electronics and Electrical Engineering. Address: Azenes 12/1, LV-1048 Riga, Latvia;

E-mail: janis.zakis@ieee.org.