

# Overview of Impedance Source Networks for Voltage Source Inverters

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**Abstract** – This paper provides an analytical overview of different impedance sources networks. General classification and main properties of different impedance source networks and their modifications are summarized and presented.

**Index Terms** – Impedance source, Power electronic converter, Voltage source inverter

## I. INTRODUCTION

OUTPUT voltage of a Voltage Source Inverter (VSI) cannot exceed the dc source voltage [24], which is one of its drawbacks in renewable energy harvesting. Traditionally, two solutions are possible: 1) using a boost or any step-up dc-dc converter coupled with a VSI (i.e. two-stage energy conversion) [33], [34], [46], [47], [50] or 2) using the impedance source network [1], [2], [4], [31], [32], which is coupled with a VSI (i.e. one-stage energy conversion). Fig. 1 presents the schematic diagram of such systems.

In terms of losses in semiconductors, both of the solutions can be generalized as follows: in the first case, VSI switches introduce the voltage stepping-up stage that consists of passive components and at least one semiconductor switch (losses in the switch) and diode (diode losses). The output voltage can be reduced or increased depending on the input voltage level. In the second case, the VSI is coupled with passive components and a diode (diode losses). Similarly, the output voltage can be regulated to obtain rated voltage level in the output. Moreover, the inverter leg short circuit problem can be overcome. In the presence of an additional switch in the boost dc-dc converter, the Z-Source Network (ZSN) is preferable.

Fig. 2a presents the Z-Source Inverter (ZSI) proposed by F.Z. Peng in 2002 [1], [2]. This unique circuit has different areas of application: energy generation systems with renewables [10], [11], [12], [14], [30], [31], [32], systems without energy storage [16]-[18] and with energy storages [12]-[14], grid connected systems [15], [19] and many other systems. These applications are possible due to the extended regulation range of the input voltage of that converter.

As discussed earlier, the ZSN contains no switching devices. This network is employed by an inverter which is coupled with a ZSN. Thanks to ZSN properties, the control algorithm of the inverter can include Shoot-Through (ST) state (simultaneous conduction of both inverter switches of

the same leg). In that interval, either one or all phase legs of the inverter can be short-circuited, which is a distinctive feature of that type of converters. However, the drawback of the ZSN is DIC essential for some applications (e.g. fuel cell). Fig. 2b presents the Quasi-Z-Source Network (qZSN) [3] as a derivation from the ZSN first presented in 2008. This circuit has continuous input current. Since that time, many varieties of impedance circuits have appeared [5].

The aim of this paper is to review Impedance Source Networks (ISN) coupled with a VSI.

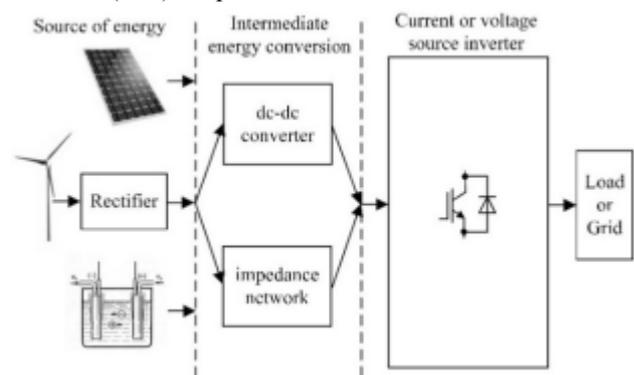


Fig. 1. Schematic diagram.

## II. DESCRIPTION OF SCHEMES

All ISNs can be subdivided into the following groups: those including inductive components [6], [9], [20] (Fig. 2 a-c), magnetically coupled inductive components (Fig. 2 d-f, k) [7], [8], [21], [23] [25]-[27], [30], [36], and including a transformer (Fig. 2 g-i, j) [22], [28]-[30]. Implementation of magnetically coupled transformers in the ISN can result in higher voltage boost factor due to the turns ratio. The impedance networks can roughly be divided (Table I) as follows: those with Discontinuous Input Current (DIC) (Fig. 2a, d, g, i, j and k) and Continuous Input Current (CIC) (Fig. 2b, c, e, f and h).

In general, an impedance source inverter operates in two operation modes – like a conventional VSI and a step-up converter.

ISNs have two main operation modes. If the input voltage is higher or equal to the nominal level, then the inverter operates like a conventional VSI (modulation index is  $M$

$\leq I$ ). If the input voltage level is below nominal, the VSI operates in a ST mode in order to boost the input voltage level. Accordingly, a switching cycle consists of three periods:  $T_a$  – non-ST state (active state) period;  $T_z$  – zero state. Zero state period can be equal to the ST period ( $t_s$ ) or equal to the sum of ST and zero ( $t_z$ ) periods.

The relative duration of the ST state is defined as:

$$D = t_s / T. \tag{1}$$

TABLE I  
CLASSIFICATION OF THE ISNS

	Separate inductors	Coupled inductors	Transformers
DIC	Z-source	T(trans)-Z-source Y-source TZ-source	LCCT-Z-source $\Gamma$ -Z-source
CIC	Quasi-Z-source EZ-source	EZ-source T(trans)- quasi-source T(trans)- quasi-source with CCM	LCCT quasi-Z-source

A. Z-Source and Quasi Z-Source Network

ZSN and qZSN [1]-[4] belong to the topologies that can comprise single magnetic components as well as coupled magnetic components [49], which results in the reduced core

losses, core size, winding losses and losses in the number of turns. Fig. 2a and Fig. 2b present these topologies. The ZSN and the qZSN consisting of two inductors  $L_1$  and  $L_2$ , two capacitors  $C_1$  and  $C_2$ , and one diode  $D_1$  are coupled with the inverter dc-link. A ZSI has DIC, a qZSI – continuous. During the ST state, the diode is not conducting in the both topologies. The energy is stored in the inductor. The dc voltage is zero. At the non-ST state, the diode is conducting. The energy of the inductance is transferred to the load and the capacitor. The boost factor ( $B$ ) of both schemes is defined as:

$$B = \frac{V_{DC}}{V_{IN}} = \frac{1}{1 - 2 \cdot D}. \tag{2}$$

Voltage stress of the ZSI on the capacitors  $C_1$  and  $C_2$  can be defined as:

$$V_{C1} = V_{C2} = V_N \cdot \frac{(1-D)}{1-2 \cdot D} = V_C. \tag{3}$$

Voltage stress of the qZSI on the capacitor  $C_1$  is defined as (3) and  $C_2$  is defined as:

$$V_{C2} = V_{IN} \cdot \frac{D}{1 - 2 \cdot D} = V_C - V_{IN}. \tag{4}$$

Voltage stress on the semiconductors can be defined as:

$$V_D = V_{IN} \cdot \frac{1}{1 - 2 \cdot D}. \tag{5}$$

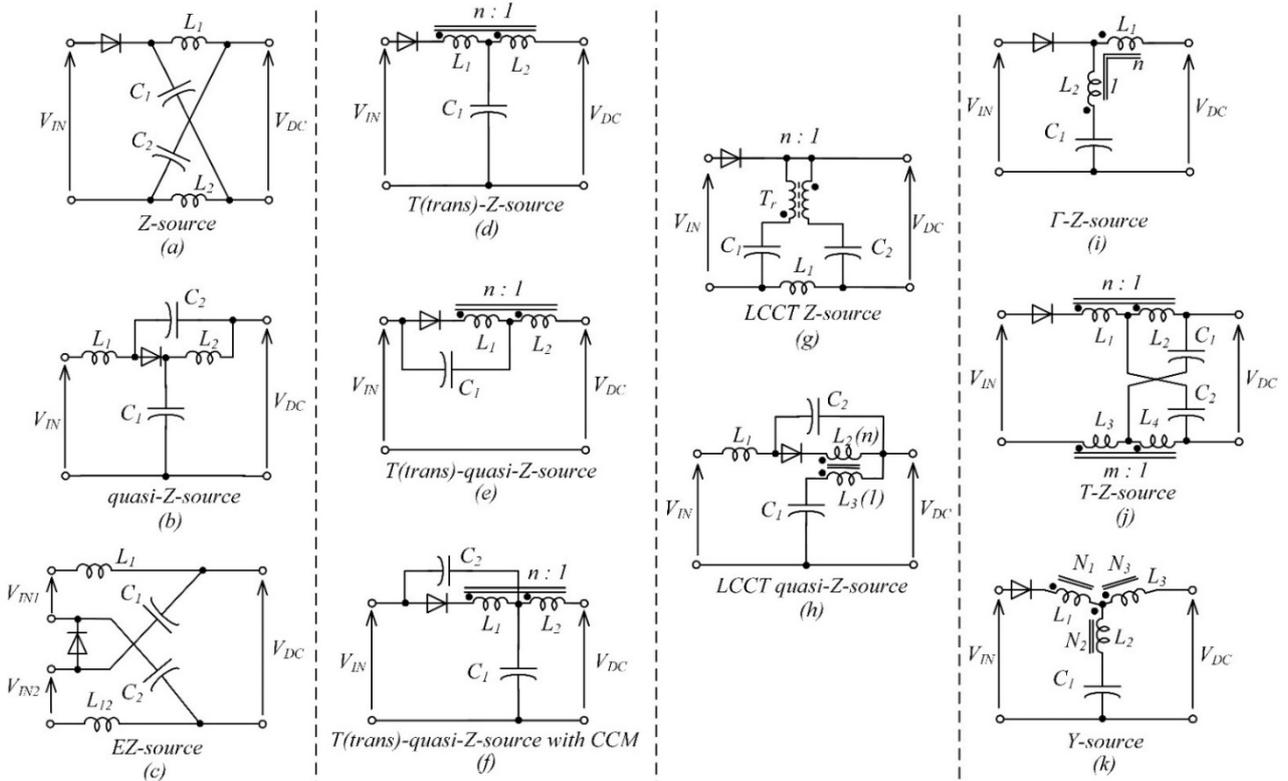


Fig. 2. Impedance source networks.

### B. EZ-Source Network

Fig 2c presents the EZ-source or Embedded Z-source network shown in [6], [9], [20]. This network has no magnetic components. It has CIC. This topology is featured by the application of multiple independent voltage sources, which is an advantage (PV panels, fuel cells), as well as a disadvantage for an EZ-source network. Additionally, a disadvantage of the network is asymmetrical working at the asymmetrical input voltage. An EZ-source network can be used in a system with energy storage. The boost factor of the circuit is expressed as (2). Voltage stress on the capacitor  $C_1$  is defined as (2) and  $C_2$  is defined as (4), where  $V_N = V_{N1} \cdot 2$ . Voltage stress on the semiconductors is defined as (5). In the EZ-source network, the voltage and current ripple is not as large as in the Z-Source inverter. Inductors  $L_1$  and  $L_2$  are applied as input current filters (i.e. external LC filters are not used). Moreover, an inductive element is placed along all the current paths in the dc frontend, the switches from the same phase leg can usually be turned ON simultaneously to introduce a ST state without damaging semiconductor devices [5].

### C. T(trans)-Z-Source, T(trans)-Quasi-Z-Source Network and T(trans)-Quasi-Z-Source Network with CCM

T(trans)-Z-source (Fig. 2d) [26], T(trans)-quasi-Z-source network (Fig. 2e) [24], and T(trans)-quasi-Z-source network with Continuous Conduction Mode (CCM).

CCM (Fig. 2f) [25] have magnetic components. It is a two-winding dual inductor  $L_1$  and  $L_2$ . The circuit is composed of two capacitors  $C_1$  and  $C_2$ , and one diode  $D_1$ . T(trans)-Z-source network has DIC, T(trans)-quasi-Z-source network with CCM – continuous. These circuits have a higher boost factor than the previous circuits and can be defined as:

$$B_1 = \frac{1}{1 - (n+1) \cdot D}. \quad (6)$$

If  $n=1$ , then B is similar to that in the previous circuits. In the T(trans)-Z-source network the coupled inductors are used like an energy storage. Voltage stress on the capacitor  $C_1$  of the trans-Z-source circuits and the inverter with CCM is defined as:

$$V_{C1} = V_{IN} \cdot \frac{(1-D)}{1 - (n+1) \cdot D}. \quad (7)$$

Voltage stress on the T(trans)-quasi-Z-source circuit on the capacitors  $C_1$  and  $C_2$  T(trans)-quasi-Z-source circuit with CCM is defined as:

$$V_{C1} = V_{IN} \cdot \frac{n \cdot D}{1 - (n+1) \cdot D}. \quad (8)$$

$$V_D = V_{IN} \cdot \frac{n}{1 - (n+1) \cdot D}. \quad (9)$$

The disadvantage of this scheme is the presence of the leakage inductance.

### D. LCCT Z-Source and LCCT Quasi-Z-Source Networks

LCCT Z-source circuit is an inductor-capacitor-capacitor-transformer Z-source circuit. LCCT Z-source and quasi-Z-source [7], [28], [29], [30] circuits are shown in Figs. 2g and 2h, respectively. These schemes include a high frequency ideal transformer. Theoretically, the topology of the LCCT circuit helps to prevent the transformer core from saturation [29]. Only one inductive element is used to store the energy during the boost operation.

LCCT Z-source circuit has DIC. LCCT quasi-Z-source circuit has CIC. The boost factor of the circuit is expressed as (6). Voltage stress on the capacitors  $C_1$  and  $C_2$  is defined as (7) and (8), respectively. Voltage stress on the semiconductors is defined as (9). The LCCT quasi-Z-source circuit combines high gain with a CIC even at low load. It is filtered to the high frequency ripple of the input current, but the input inductor is required. LCCT circuit can be further optimized using higher switching frequency semiconductors such as SiC diodes.

### E. F-Z-Source Network

F-Z-source network [22], [33], [33] contains a transformer. The circuit is shown in Fig. 2i. F-Z-source circuit has DIC. The boost factor of the circuit is defined as:

$$B_2 = \frac{1}{1 - \frac{n}{n-1} \cdot D}. \quad (10)$$

If  $n=1$ , then B is like in the Z-source circuit. However, unlike that, in the F-Z-source circuit, only one capacitor is applied. Voltage stress of F-Z-source inverters on the capacitor  $C_1$  is defined as:

$$V_{C1} = V_{IN} \cdot \frac{(1-D)}{1 - \frac{n}{n-1} \cdot D}. \quad (11)$$

Voltage stress on the semiconductors is defined as:

$$V_D = V_{IN} \cdot \frac{1}{n \cdot (1-D) - 1}. \quad (12)$$

The disadvantage of this scheme is the presence of the leakage inductance which may influence on the voltage and current stress over semiconductors.

### F. T-Z-Source Network

T-Z-source network [26] scheme contains magnetic components. It is a two-winding dual inductor. T-Z-source network has DIC. This circuit has a higher boost factor than the previous circuits because of the turn ratio of the coupled inductor. The boost factor of circuit is defined as:

$$B_3 = \frac{1}{1 - (2+n+m) \cdot D}. \quad (13)$$

Voltage stress on the capacitor  $C_1$  is defined as:

$$V_{C1} = V_{IN} \cdot \frac{(1+n+m) \cdot D}{1-(2+n+m) \cdot D} \quad (14)$$

Voltage stress on the semiconductors is defined as:

$$V_D = V_{IN} \cdot \frac{1+n+m}{1-(2+n+m) \cdot D} \quad (15)$$

In the circuit, resonant effects can occur. Because of that, the transient currents can be substantial. Additionally, this circuit consists of the elements, the number of which is higher than in the other schemes, but the input current is discontinuous.

G. FY-Source Network

Y-source network [36] belongs to the schemes with magnetically coupled components. It is a three-winding inductor. The circuit is shown in Fig. 2k. Y-source network has DIC. The boost factor of circuit is defined as:

$$B_4 = \frac{1}{1-\left(\frac{N_3+N_1}{N_3-N_2}\right) \cdot D} \quad (16)$$

Voltage stress on the capacitor  $C_1$  is defined as:

$$V_{C1} = V_{IN} \cdot \frac{1-D}{1-\left(\frac{N_3+N_1}{N_3-N_2}\right) \cdot D} \quad (17)$$

Voltage stress on the semiconductors is defined as:

$$V_D = V_{IN} \cdot \frac{\frac{N_3+N_1}{N_3-N_2} - 1}{1-\left(\frac{N_3+N_1}{N_3-N_2}\right) \cdot D} \quad (18)$$

The disadvantage of this scheme is the presence of the leakage inductance. Possible wide class of the converters based on this network is presented in [36]. However, buck mode was not experimentally verified.

III. OTHER MODIFICATIONS

Modifications based on the above schemes are shown in Fig. 3 [4], [40], [46]. The most common method is to use a switched inductor, as shown in Fig. 3a [37], [38], [42]. This is derived by replacing the inductor  $L_2$  in the qZSN by one of the switched inductors, shown in Fig. 3a [40]. In [27] cascaded TZ-source inverters are discussed.

The second type of modification called capacitor assisted extended boost (CAEB) [39], [41] is shown in Fig. 3b and modified capacitor assisted extended boost (MCAEB) [39], [41] is shown in Fig. 3c. CAEB is derived by adding one diode ( $D_2$ ), one inductor ( $L_3$ ) and two capacitors ( $C_3$  and  $C_4$ ) to the traditional qZSI. MCAEB is derived from the CAEB qZSI by changing the connection points of the capacitors  $C_2$  and  $C_3$  [40].

The third type of modification called diode assisted extended boost (DAEB) [45] is shown in Fig. 3d, and a modified diode assisted extended boost (MDAEB) [45] is shown in Fig. 3e. DAEB is derived by adding one capacitor ( $C_3$ ), one inductor ( $L_3$ ) and two diodes ( $D_2$  and  $D_3$ ) to the traditional qZSI. MDAEB is derived from the DAEB qZSI by changing the connection points of the capacitor  $C_3$ .

Theoretically, these modifications can produce infinite boost [42]. However, this cannot occur in practice due to losses. Out of the modifications, CAEB is preferable, since it

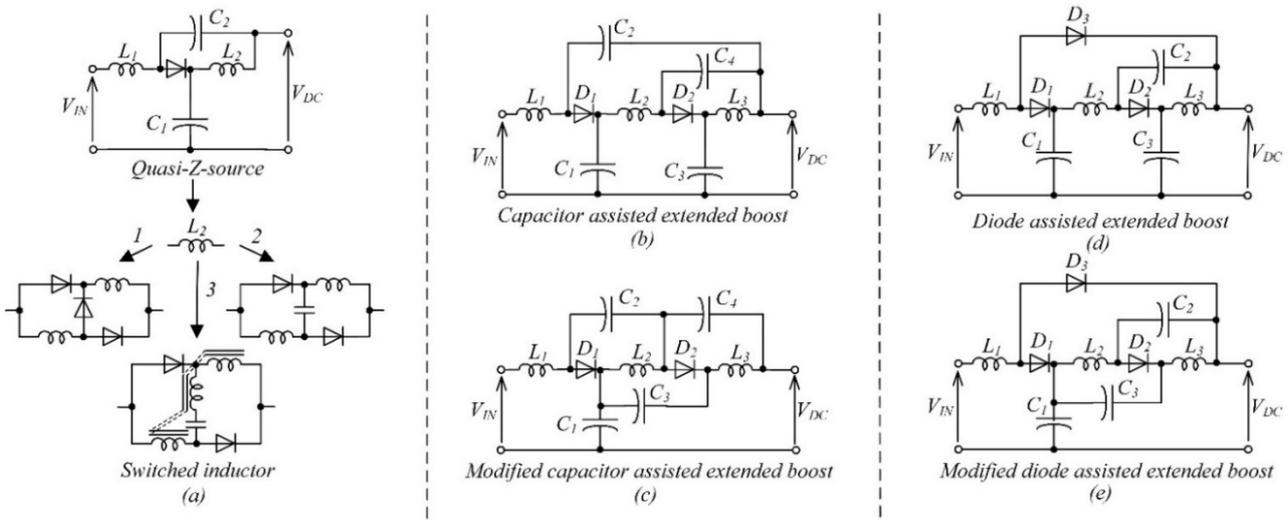


Fig. 3. Other modifications.

TABLE II  
BASIC PROPERTIES AND EXPRESSIONS OF IMPEDANCE SOURCE NETWORKS

Fig.	Name	Boost (B)	$V_{C1}^*$	$V_{C2}^*$	$V_D$	CIC	Properties of the circuit	
2a	Z-source	$B$ $\frac{1}{1-2 \cdot D}$	$\frac{1-D}{1-2 \cdot D}$	$\frac{1-D}{1-2 \cdot D}$	$\frac{1}{1-2 \cdot D}$	-	+ first circuit	
2b	Quasi-Z-source		$\frac{1-D}{1-2 \cdot D}$	$\frac{D}{1-2 \cdot D}$		+ + continuous input current $i_{IN}$		
2c	EZ-source		$\frac{1-D}{1-2 \cdot D}$	$\frac{D}{1-2 \cdot D}$		+ +/– several dc input current sources – asymmetry if $U_{IN1} \neq U_{IN2}$ + lower inductor L voltage ripple – more inductor L current ripple		
2d	T(trans)-Z-source	$B_1$ $\frac{1}{1-(n+1) \cdot D}$	$\frac{1-D}{1-(n+1) \cdot D}$	---	$\frac{n}{1-(n+1) \cdot D}$	-	+ one capacitor + small size passive components	
2e	T(trans)-quasi-Z-source		$\frac{n \cdot D}{1-(n+1) \cdot D}$	---		+ + one capacitor – large input current ripple		
2f	T(trans)-quasi-Z-source with CCM		$\frac{1-D}{1-(n+1) \cdot D}$	$\frac{n \cdot D}{1-(n+1) \cdot D}$		+ + smoother input current $i_{IN}$		
2g	LCCT Z-source		$\frac{1-D}{1-(n+1) \cdot D}$	$\frac{n \cdot D}{1-(n+1) \cdot D}$		- - discontinuous input current $i_{IN}$		
2h	LCCT quasi-Z-source		$\frac{1-D}{1-(n+1) \cdot D}$	$\frac{n \cdot D}{1-(n+1) \cdot D}$		+ + no need for filter of input current – more passive components		
2i	$\Gamma$ -Z-source	$B_2$ $\frac{1}{1-\frac{n}{n-1} \cdot D}$	$\frac{1-D}{1-\frac{n}{n-1} \cdot D}$	---	$\frac{1}{(n-1) \cdot \left[1-\frac{n}{n-1} \cdot D\right]}$	-	+ one capacitor – larger inductor L current ripple	
2j	T-Z-source	$B_3$ $\frac{1}{1-(2+n+m) \cdot D}$	$\frac{(1+n+m) \cdot D}{1-(2+n+m) \cdot D}$		$\frac{1+n+m}{1-(2+n+m) \cdot D}$	-	– large transient currents – larger inductor L current ripple	
2k	Y-source	$B_4$ $\frac{1}{1-\left(\frac{N_3+N_1}{N_3-N_2}\right) \cdot D}$	$\frac{1-D}{1-\left(\frac{N_3+N_1}{N_3-N_2}\right) \cdot D}$	---	$\frac{\frac{N_3+N_1}{N_3-N_2}-1}{1-\left(\frac{N_3+N_1}{N_3-N_2}\right) \cdot D}$	-	– presence of leakage inductance (current and voltage surge)	
3a	Switched-inductor 1	$B_{5,1}$ $\frac{1+D}{1-2 \cdot D-D^2}$	$\frac{1-D}{1-2 \cdot D-D^2}$	$\frac{2 \cdot D}{1-2 \cdot D-D^2}$	$\frac{1+D}{1-2 \cdot D-D^2}$	+	– leakage inductance are presence	
3a	Switched-inductor 2	$B_{5,2}$ $\frac{2}{1-3 \cdot D}$	$V_{C1}^* = V_{C3}^* = \frac{1-D}{1-3 \cdot D}$	$\frac{1+D}{1-3 \cdot D}$	$\frac{2}{1-3 \cdot D}$	+		
3a	Switched-inductor 3 $n=1$	$B_{5,3}$ $\frac{3}{1-4 \cdot D}$	$V_{C1}^* = \frac{V_{C3}^*}{2} = \frac{1-D}{1-4 \cdot D}$	$\frac{2+D}{1-4 \cdot D}$	$\frac{3}{1-4 \cdot D}$	+		
3b	CAEB	$B_6$ $\frac{1}{1-3 \cdot D}$	$V_{C1}^* = \frac{1-2 \cdot D}{1-3 \cdot D}$ , $V_{C3}^* = \frac{1-D}{1-3 \cdot D}$	$V_{C2}^* = \frac{2 \cdot D}{1-3 \cdot D}$ , $V_{C4}^* = \frac{D}{1-3 \cdot D}$	$\frac{1}{1-3 \cdot D}$	+		– number of passive components increased – more diodes + less voltage stress of diodes + higher boost factor
3c	MCAEB		$V_{C1}^* = \frac{1-2 \cdot D}{1-3 \cdot D}$	$V_{C2}^* = V_{C3}^* = V_{C4}^* = \frac{D}{1-3 \cdot D}$		+		
3d 3e	DAEB MDAEB	$B_7$ $\frac{1}{(1-2 \cdot D) \cdot (1-D)}$	$\frac{1}{(1-D)}$	$V_{C2}^* = V_{C3}^* = \frac{D}{1-2 \cdot D} \cdot V_{C1}^*$	$V_{D1} = V_{D3} = (1-D) \cdot B_7$ $V_{D2} = \frac{1}{(1-2 \cdot D) \cdot (1-D)}$	+		

requires fewer semiconductor devices. Therefore, the circuit may have lower power losses.

All of these modification types are limited in practical solutions. These schemes contain many passive components and have additional losses in the semiconductors.

#### IV. COMPARATIVE ANALYSIS

Table II summarizes previously discussed impedance source topologies. Legend to table:  $B$  – boost factor (for

each scheme  $B_n$ );  $V_{Cn}^*$  – capacitor voltage relative to the input voltage  $V_{IN}$ ;  $V_D$  – semiconductors voltage relative to  $V_{IN}$ . Assuming that  $n=N_3/N_1=N_3/N_2=2$  is an equal value for all circuits, Fig. 4 illustrates the boost factor dependencies as a function of the relative duration of the ST state. As the graphs show, with an increase in the relative duration of the ST state  $D$ , the boost factor increases.

Switched-inductor 3, T-Z-source and switched-inductor 2 are the largest of the remaining boost factor. The smallest gain is at the Z-source and  $\Gamma$ -Z-source circuits.

Fig. 5 illustrates the boost factor dependencies as a function of the turn ratio factor  $n=N_3/N_1=N_3/N_2$ . On the interval  $n<1.5$   $\Gamma$ -Z-source, the Y-source circuits have the highest boost factor. However, TZ-source circuit has the highest boost factor for  $n>1.5$ . It is quite a high boost factor for both T(trans)-Z-source circuits and LCCT Z-source circuits.

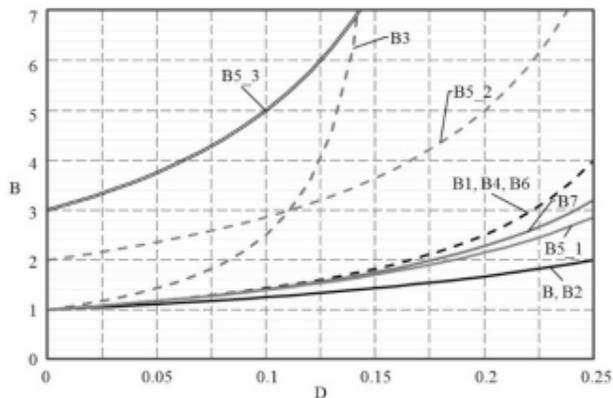


Fig. 4. The boost factor as a function of the relative duration of the ST state.

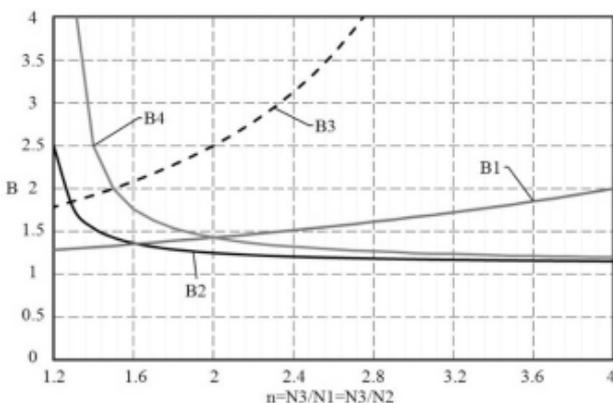


Fig. 5. The boost factor as a function of the turn ratio factor  $n$ ,  $D=0.1$ .

## V. CONCLUSIONS

Existing ISNs were analyzed. The analysis showed that all networks have advantages and disadvantages. It can be concluded that T-Z-source circuit is the network with the smallest number of the passive elements and with the highest boost factor. However, it is limited for  $D<0.15$ . Moreover, a circuit has a steep characteristic ( $B=f(D)$ ) at  $0.11<D<0.15$ . It can be assumed that the feedback control system for this circuit is complicated because the voltage gradient  $\Delta B$  at  $0.11<D<0.15$  will be very large. T(trans)-Z-source circuits, LCCT Z-source circuits, Y-source circuit, CAEB circuits and switched-inductor 2 have a high boost factor and fairly smooth characteristics. Additionally, LCCT quasi-Z-source circuit is preferable because it has CIC and high boost. Moreover, it has simple practice realization comparing to DAEB, CAEB, switched-inductor topologies or Y-source network.

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