IET Power Electronics

Research Article

IET Journals
The Institution of Engineering and Technology

LCCT-derived three-level three-phase inverters

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Abstract: Solutions for a family of the novel three-level neutral-point-clamped (NPC) inductor-capacitor-capacitor-transformer (LCCT)-derived three-phase inverters are described and compared. Component design guidelines and steady state analysis, current and voltage waveforms are given. The authors' simulation results confirm the theoretical predictions. It was found that an asymmetrical three-level NPC LCCT-derived inverter with a single diode in the impedance source network is the most promising solution. Experimental results for an asymmetrical three-level NPC LCCT-derived inverter with a single input voltage source and continuous input current are presented. The main advantages and design requirements are discussed.

1 Introduction

Renewable energy sources have become a key area in the advancement of modern power electronics [1]. In the photovoltaic systems, several configurations are used. Among the technologies, the string technology is very popular due to its low cost and simplicity [2, 3]. However, one of the major drawbacks of the string technology is poor energy utilisation at partial shadowing or high operating temperature. It leads to a wide range of input voltage variations. Traditionally, voltage source inverters or current source inverters cannot provide higher than a double input voltage regulation ratio. To overcome that drawback, intermediate voltage boost dc–dc converters are used. At the same time, this solution is topologically more complex and harder to control because of the two-stage power conversion.

Recent solutions based on the impedance-source (IS) networks have been extended to various application areas. Z-Source inverters (ZSIs) and their derivations were proposed as promising solutions for single stage dc–ac applications [4–9]. Since then, many topological derivations have been proposed and recently a number of review papers have been published [10–12].

Modular and multilevel converter applications are a novel trend in power electronics. Multilevel converters have major advantages over the conventional and well-known two-level converters. These advantages lie in improved output power quality and higher nominal power in the converter and lower demands to the filters [13–16]. Today's multilevel converters are a good solution for low power and low voltage applications as well. Reduced voltage stress allows using fast MOSFET semiconductors in industrially verified Si technologies. The thee-level (3L) ZSI was proposed in [12] as a logical extension of the two-level inverter and the ZSI. The combination of any IS networks with multilevel or cascaded inverters enables single-stage energy conversion with the buck-boost capability. Comprehensive studies of 3L neutral-point-clamped (NPC) quasi-ZSI (qZSI) are covered in [17, 18]. The proposed solution combines the above-mentioned advantages along with continuous input current (CIC).

At the same time, the use of a pure dc-link is the main problem of ZSI and qZSI. To overcome this problem, IS networks based on coupled inductors have been proposed [19–25]. In addition, 3L NPC solutions are discussed in [21, 26]. Existing multilevel solutions based on IS networks are analysed in [27]. It is shown that solutions with coupled inductors may provide better dc-link utilisation along with the reduced capacitor size. A similar effect can be achieved by means of IS networks with an ideal transformer. A common drawback of any IS solution based on the coupled inductors lies in the leakage inductance, which leads to the current and voltage spikes on the semiconductors [21] along with reduction in the effective ST duty cycle. As a result, it requires more precise design of magnetics.

Fig. 1 shows the family of the inductor-capacitor-capacitor-transformer (LCCT)-source networks as proposed in [27]. LCCT Z-source (Fig. 1*a*) and LCCT Z-source with CIC (Fig. 1*b*) are based on the ideal transformer with zero instantaneous flux, while LCCT qZ-source network (Fig. 1*c*) has a coupled inductor.

It has demonstrated improved performance compared with the trans-Z-source and T-source inverters reported recently. The proposed topologies characterise available CIC even during light-load operation. The negative impact of the parasitic parameters of the coupled inductors on the dc-link voltage is significantly reduced. This idea is developed further in [28–30]. Thanks to the unique topology of the input impedance network, the LCCT-Z-source inverter may achieve ripple- free input current.

This paper presents three-phase 3L NPC inverter solutions based on the LCCT networks. Simulation and experimental results for several novel topologies have confirmed theoretical predictions. Pros and cons are also discussed in the paper.

2 Proposed 3L LCCT-derived inverters

Fig. 2 shows the proposed three-phase 3L LCCT-derived NPC inverters. These topologies are based on the introduction of the high-frequency transformer and additional capacitors. A Z-source NPC inverter with a single impedance network presented in [31–33] could be supplied from a single input voltage source (Fig. 2*a*). Fig. 2*b* illustrates a similar solution with a double transformer and a separate input voltage dc source. A common drawback of these solutions is a discontinuous input current. Fig. 2*c* demonstrates a

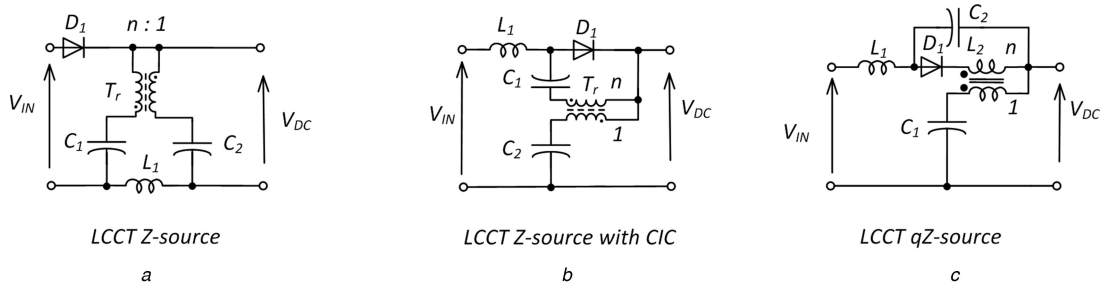

Fig. 1 *Existing LCCT-source networks*
(a) Z-source, ***(b)*** Z-source with CIC, ***(c)*** qZ-source

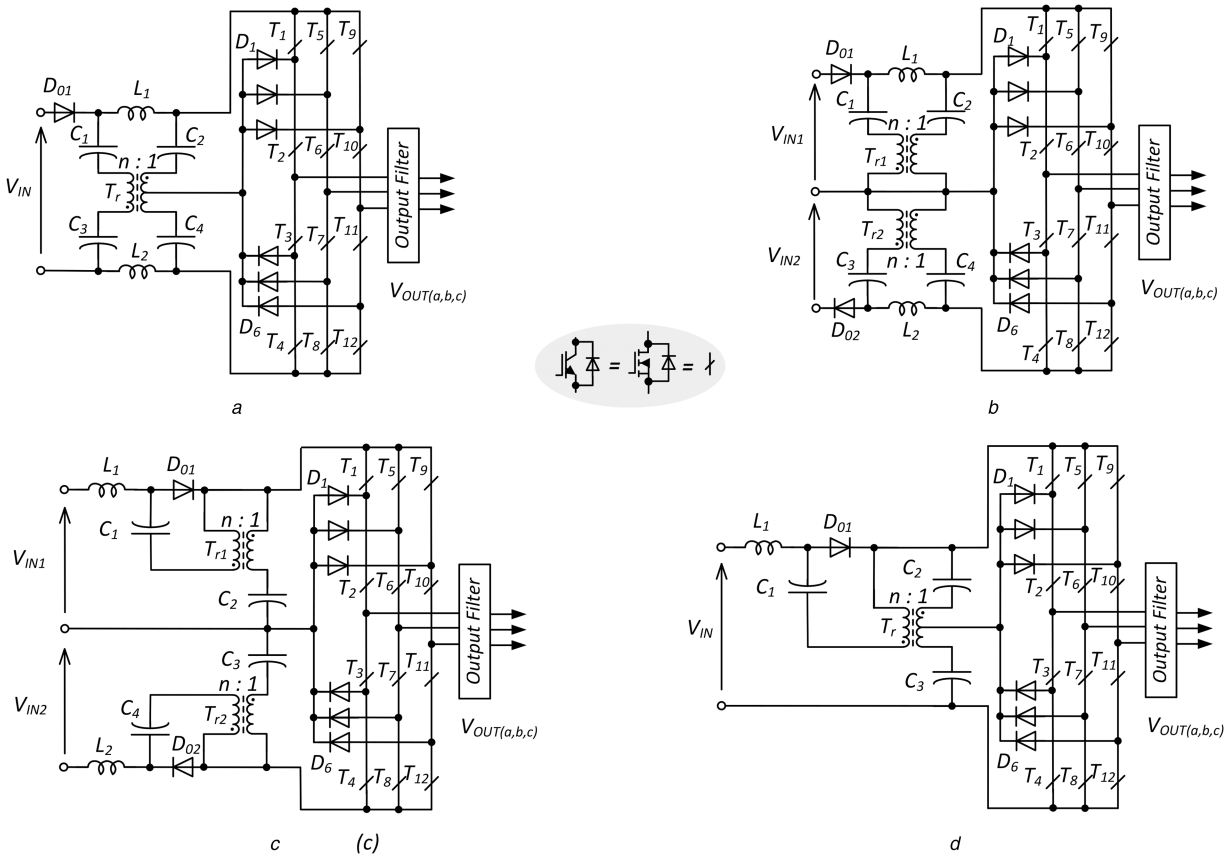

Fig. 2 *Three-phase 3L LCCT-derived NPC inverters*
(a) 3L NPC LCCT Z-source network with a single input voltage source, ***(b)*** 3L NPC LCCT Z-source network with separated input voltage sources, ***(c)*** 3L NPC LCCT Z-source network with separated input voltage sources and CIC, ***(d)*** 3L NPC LCCT Z-source network with a single input voltage source and CIC

novel symmetrical LCCT-derived 3L three-phase NPC inverter with CIC. It is based on the LCCT network presented in [28]. Due to the separated input voltage, dc source solutions depicted in Figs. 1*b* and *c* are not sensitive to an unbalanced three-phase load. At the same time, it is evident that these solutions have two diodes in the impedance networks that may decrease the overall converter efficiency. It was shown in [18] that with a string photovoltaic 3L NPC qZSI, the voltage drop across the two IS diodes leads up to 30% of the overall losses.

Fig. 2*d* demonstrates a novel LCCT-derived 3L NPC inverter with a single input voltage dc source, a minimum number of passive components, a single IS diode, and CIC.

It is evident that all the derived topologies have the same boost factor *B* presented in [11]:

$$B = \frac{V_{\mathrm{DC}}}{V_{\mathrm{IN}}} = \frac{1}{1-(1+n)\cdot D_S}. \qquad (1)$$

At the same time, the proposed topologies have different amounts of passive components. Another issue to be emphasised is the presence of the ideal transformer. To avoid its saturation, the total magnetic flux must be equal to zero. This specific condition will be studied for three-winding transformers where the central tap is connected to the neutral wire of the NPC converter.

For our comparison, component design must be analysed in terms of their overall size, current and voltage stress.

3 Component design GuidElines

To compare component design in terms of their overall size, full steady state analysis will be performed in this section. The approach will be demonstrated for the topology in Fig. 2*d*. Similar results for other solutions are summarised in Table 1.

In this step, several assumptions should be mentioned. In this topology, a transformer is considered ideal, i.e. without leakage inductance. Further, only a symmetrical three-phase system is considered; as a result, neutral wire current is negligible.

Fig. 3 illustrates the equivalent circuits of the 3L LCCT-derived topology presented last. In particular, Fig. 3*a* corresponds to the shoot-through (ST) states when all the transistors are conducting. Fig. 3*b* corresponds to the active states.

In the analysis, the following parameters were used: $v(t) = v$ – instantaneous value of the variable; $\langle v \rangle_T$ – average value of the variable for the time period; V – peak value of the variable. Finally,

Table 1 Comparison of the passive elements of the three-phase 3L LCCT-derived NPC inverters

Topology	Inductors			Capacitors		
	No.	Average current	Value	No	Average voltage	Value
3L NPC LCCT Z-source network, (Figs. 2*a* and *b*	L_1, L_2	$\frac{P}{V_{IN}}$	$\frac{V_{IN}^2 \cdot D \cdot T \cdot (1-D) \cdot (1+n)}{2 \cdot k_L \cdot P \cdot (1-(n+1) \cdot D)} \cdot \left(\frac{1-D}{n \cdot D}\right)$	C_1, C_4	$\frac{V_{IN} \cdot D \cdot n}{2 \cdot (1-(n+1) \cdot D)}$	$\frac{2 \cdot P \cdot T \cdot (1-(n+1) \cdot D)}{k_1 \cdot V_{IN}^2 \cdot n}$
				C_2, C_3	$\frac{V_{IN} \cdot (1-D)}{2 \cdot (1-(n+1) \cdot D)}$	$\frac{2 \cdot P \cdot T \cdot (1-(n+1) \cdot D) \cdot D}{k_2 \cdot V_{IN}^2 \cdot n \cdot (1-D)}$
3L NPC LCCT Z-source network, (Fig. 2*c*)	L_1, L_2	$\frac{P}{V_{IN}}$	$\frac{V_{IN}^2 \cdot D \cdot T \cdot (1-D) \cdot (1+n)}{2 \cdot k_L \cdot P \cdot (1-(n+1) \cdot D)} \cdot \left(\frac{1-D}{n \cdot D}\right)$	C_1, C_4	$\frac{V_{IN} \cdot D \cdot n}{2 \cdot (1-(n+1) \cdot D)}$	$\frac{2 \cdot P \cdot T \cdot (1-(n+1) \cdot D)}{k_1 \cdot V_{IN}^2 \cdot n}$
				C_2, C_3	$\frac{V_{IN} \cdot (1-D)}{2 \cdot (1-(n+1) \cdot D)}$	$\frac{2 \cdot P \cdot T \cdot (1-(n+1) \cdot D) \cdot D}{k_2 \cdot V_{IN}^2 \cdot n \cdot (1-D)}$
3L NPC LCCT Z-source network, (Fig. 2*d*)	L_1	$\frac{P}{V_{IN}}$	$\frac{V_{IN}^2 \cdot D \cdot T \cdot (1-D) \cdot (1+n)}{k_L \cdot P \cdot (1-(n+1) \cdot D)} \cdot \left(\frac{1-D}{n \cdot D}\right)$	C_1	$\frac{V_{IN} \cdot D \cdot n}{1-(n+1) \cdot D}$	$\frac{P \cdot T \cdot (1-(n+1) \cdot D)}{k_1 \cdot V_{IN}^2 \cdot n}$
				C_2, C_3	$\frac{V_{IN} \cdot (1-D)}{2 \cdot (1-(n+1) \cdot D)}$	$\frac{2 \cdot P \cdot T \cdot (1-(n+1) \cdot D) \cdot D}{k_2 \cdot V_{IN}^2 \cdot n \cdot (1-D)}$

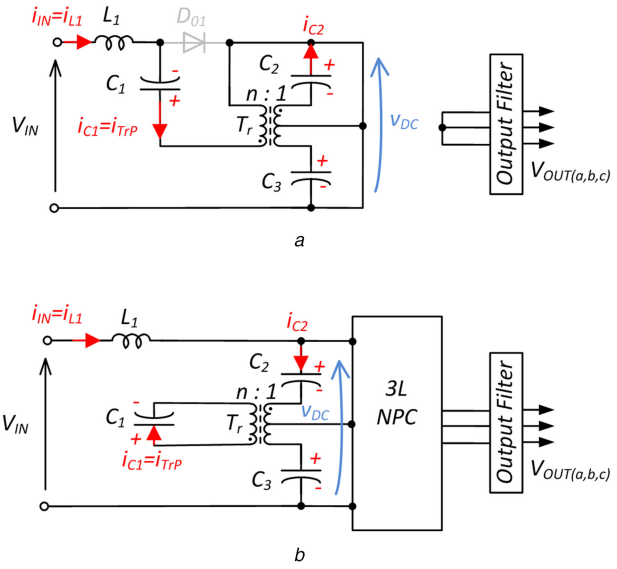

Fig. 3 *Equivalent circuits of the novel LCCT-derived 3L NPC inverter*
(a) For ST state, ***(b)*** Active state

all the time intervals were defined, as shown in Fig. 4 and denoted as: T_S – ST state time period; T_a – non-ST state (active state) time period; T – switching period.

From the voltage balance across the inductors $\langle v_{L1} \rangle_T = 0$, the voltage across the capacitors C_1, C_2, C_3 can be defined as:

$$\langle v_{C1} \rangle_T = \frac{V_{IN} \cdot D \cdot n}{1-(n+1) \cdot D}, \quad D = \frac{T_S}{T}, \tag{2}$$

$$\langle v_{C2} \rangle_T = \langle v_{C3} \rangle_T = \frac{V_{IN} \cdot (1-D)}{2 \cdot (1-(n+1) \cdot D)}, \tag{3}$$

where V_{IN} – input voltage; v_{C1}, v_{C2}, v_{C3} capacitors voltage; n – turns ratio of the transformer and D is the ST duty cycle.

To define the capacitance value, it is necessary to determine the current pulse over the capacitor. The current of the capacitor C_1 during the ST state is defined as:

$$\langle i_{C1} \rangle_{T_s} = C_1 \cdot \frac{dv_{C11}}{dt} = \langle i_{IN} \rangle_{T_s}. \tag{4}$$

The voltage ripple on the capacitor C_1 can be derived as:

$$\Delta V_{C1} \le k_1 \cdot \langle v_{C1} \rangle_T = \frac{1}{C_1} \int_0^{T_S} \langle i_{C1} \rangle_{T_s} \cdot dt, \tag{5}$$

where k_1 – voltage ripple factor of the capacitor C_1.

Assuming an ideal case without losses, it can be claimed that the average input power and output power are equal:

$$\langle P_{IN} \rangle_T = \langle P_{dc} \rangle_T = P. \tag{6}$$

The average input current ($\langle i_{IN} \rangle_T$) can be derived as:

$$\langle i_{IN} \rangle_T = \frac{P}{V_{IN}}. \tag{7}$$

Finally, from (2), (4), (5) and (7), the capacitor C_1 can be calculated as:

$$C_1 \ge \frac{P \cdot T \cdot (1-(n+1) \cdot D)}{k_1 \cdot V_{IN}^2 \cdot n}. \tag{8}$$

By means of a similar approach, the value of the capacitors C_2, C_3 can be defined as:

$$C_2 = C_3 \ge \frac{2 \cdot P \cdot T \cdot (1-(n+1) \cdot D) \cdot D}{k_2 \cdot V_{IN}^2 \cdot n \cdot (1-D)}, \tag{9}$$

where k_2 – voltage ripple factor of the capacitors C_2, C_3.

It can be seen that the capacitor values C_2, and C_3 increase with the ST duty cycle increasing. It means that the boost operation mode requires larger capacitor value, while the buck operation mode requires no capacitors. At the same time, capacitor C_1 has opposite dependences. Also, it should be noted that the values of all the capacitors can be reduced by means of the turns ratio n increased.

The equations for the inductor voltage and current ripple during the active state (T_a) are derived as:

$$L_1 \cdot \frac{di_{L1}}{dt} = \langle v_{L1} \rangle_{T_a} = V_{DC} - V_{IN}, \tag{10}$$

$$\Delta i_{L1} = \frac{1}{L_1} \int_0^{T_a} (V_{DC} - V_{IN}) \cdot dt. \tag{11}$$

It is taken into account that the average input current is equal to the inductor current $\langle i_{L1} \rangle_T = \langle i_{IN} \rangle_T$ and the boundary conduction mode:

$$\frac{\Delta i_{L1}}{2} \le \langle i_{L1} \rangle_T. \tag{12}$$

Using (1), (7), (11), the expression for the inductor L_1 is

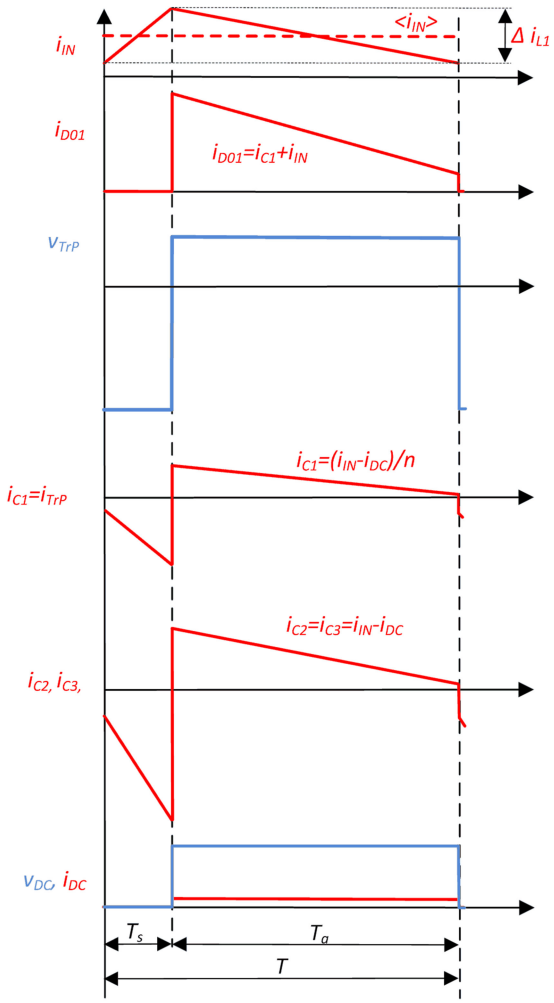

Fig. 4 *Idealised current and voltage waveforms of the novel LCCT-derived 3L NPC inverter shown in Fig. 2d*

$$L_1 \geq \frac{V_{IN}^2 \cdot D \cdot T \cdot (1-D) \cdot (1+n)}{k_L \cdot P \cdot (1-(n+1) \cdot D)}, \tag{13}$$

where k_L – the current ripple factor defined similar to the voltage ripple factor of the capacitors.

The final goal is to obtain expressions of the passive components value as a function of the predefined voltage ripple across the capacitors and the current ripple across the inductor. Along with average voltage on the capacitors and average current on the inductors, the relative size can be estimated.

The voltage and current waveforms across the key components are illustrated in Fig. 4.

It was assumed that voltage ripple across the capacitors is negligible. At the same time, it can be drawn an interesting conclusion: in order to provide converter performance in accordance with equivalent circuits, the capacitor C_1 current should not drop to zero during an active state. Average current i_{C1} during an active state can be estimated as:

$$\langle i_{C1} \rangle_{T_a} = \frac{\langle i_{IN} \rangle_{T_a} - \langle i_{DC} \rangle_{T_a}}{n}, \tag{14}$$

where i_{DC} is a dc-link current. Taking into account the power balance and (1), it can be written as:

$$\langle i_{C1} \rangle_{T_a} = \frac{\langle i_{IN} \rangle_{T}}{n} \cdot \left(\frac{n \cdot D}{1-D} \right). \tag{15}$$

Since the input current ripple defines the capacitor current ripple, it can be concluded that the inductance value must be increased to avoid capacitor current dropping to zero during an active state. As a result, the final expression for the inductor value should be specified as:

$$L_1' \geq \frac{V_{IN}^2 \cdot D \cdot T \cdot (1-D) \cdot (1+n)}{k_L \cdot P \cdot (1-(n+1) \cdot D)} \cdot \left(\frac{1-D}{n \cdot D} \right) \tag{16}$$

Similar analysis was performed for all the presented topologies. Table 1 summarises the results.

Our analysis showed that the topologies with discontinuous input current contain the same amount and size of passive elements and have no benefits. As a result, they were omitted from further simulation and experimental study.

4 Simulation and experimental verifications

The converter circuits were simulated in PSIM. The parameters for the simulation and experiment described in Section 3 are summarised in Table 2. To model the losses in the circuit, the very small resistance r was added in series to the inductance L_1 in the simulation model.

4.1 Simulation results

First simulation results of the topology shown in Fig. 2*c* are illustrated in Fig. 5. A very simple carrier-based modulation technique that can be applied for any 3L IS inverter was used in [34]. This modulation technique is based on the simple boost control with equally distributed ST states.

Fig. 5 demonstrates the output phase to neutral voltage, average capacitor voltages $V_{C1} = V_{C4} = 369$ V, $V_{C2} = V_{C3} = 234$ V, and the current of the middle point i_{ZERO}. This case corresponds to the input voltage $V_{IN} = 325$ V and average input current $I_{IN} = 3.7$ A. It can be seen that high-frequency oscillation is present, which may evoke voltage unbalance on the capacitors. At the same time, such ripples can be mitigated by means of a more complex modulation strategy. Output power was ~1 kW.

The second case of the simulation study corresponds to the topology shown in Fig. 2*d*. Fig. 6 demonstrates similar waveforms with the output phase to neutral voltage, capacitor average voltages $V_{C1} = 340$ V, $V_{C2} = V_{C3} = 332$ V. The current of the middle point for both networks looks the same and has the same parameters as well. The dc-link voltage in both cases is ~900 V. The output *LCL*-filter was used. The THD of the output voltage for both cases was ~5%.

In conclusion, asymmetrical 3L NPC LCCT Z-source network (Fig. 2*d*) looks more attractive because of fewer passive components and one fewer diode element in the impedance network. The input current is continuous and identical for both circuits. Previous experimental studies of the IS-derived inverters demonstrated that contributions of IS network diodes to the overall losses are substantial, which deteriorates the efficiency of the converter [18, 34]. As a result, any solutions that involve a reduced number of IS diodes are preferable.

4.2 Experimental results

To confirm the solutions above experimentally, a simple non-optimised laboratory prototype of the asymmetrical 3L NPC LCCT Z-source inverter was assembled. The types and values of the components used in the experimental prototype are presented in Table 3.

Taking into account the results above, the final passive elements for the experimental verification were chosen to provide full CCM in the whole operating range.

The control system is based on the FPGA board with EP4CE22E22C8 from Altera. The FPGA makes it easier to implement the ST state that is important for the given topology. The ACPL-H312 chosen has a cheap high-frequency unidirectional driver. High-switching frequency SiC MOSFETs with fast body diodes and SiC NPC and LCCT network diodes allow the switching frequency to be raised up to 100 kHz, which in turn reduces the size of the passive components. The passive resistor

was used as a load. The regulated dc power supply was used as input voltage source. All the measurements were made by a digital oscilloscope Tektronix DPO7254, current probes Tektronix TCP0030, and voltage probes Tektronix TPA-BNC.

Fig. 7 shows the experimental setup and the diagrams obtained. Fig. 7*a* shows an experimental prototype that includes LCCT network, 3L NPC and output filter along with a control board. The output phase to neutral sinusoidal voltage is shown in Fig. 7*b*. Finally, Fig. 7*c* summarises the experimental study of the boost factor of the proposed solution. It can be seen that the experimental boost factor is close to that mathematically predicted, which proves the quality of the obtained mathematical expressions. Some disagreement is explained by the losses in the experimental prototype.

Table 2 Components and parameters for three-phase 3L LCCT-derived inverters

Network	Symmetrical 3L NPC LCCT Z-source network (Fig. 2*c*)	3L NPC LCCT Z-source network (Fig. 2*d*)
V_{OUT} – RMS output voltage	three-phase 230 V	
D – ST duty cycle	0.2	
n – inductor turns ratio	2	
V_{IN} – input voltage	325 V	
P – output power	1000 W	
T – switching cycle	10 µs	
M – modulation index	0.8	
r – losses resistance	0.01 Ω	
C_1 – capacitor	600 µF	300 µF
C_2– capacitor	190 µF	190 µF
C_3 – capacitor	600 µF	190 µF
C_4 – capacitor	190 µF	—
L_1 – inductance	1.5 mH	3 mH
L_2 – inductance	1.5 mH	—
L_{fa1}, L_{fb1}, L_{fc1}-first output filter inductors	0.5 mH	
L_{fa2}, L_{fb2}, L_{fc2}-second output filter inductors	0.2 mH	
C_{fa}, C_{fb}, C_{fc}- output filter capacitors	0.47 µF	

Fig. 8 demonstrates detailed experimental waveforms: input voltage $V_{IN} = 160$ V and average input current $I_{IN} = 2$ A; the current of the middle point i_{ZERO} is shown along with primary V_{TrP} and secondary V_{TrS} transformer voltages, and finally, capacitor voltages $V_{C1} = 165$ V, $V_{C2} = V_{C3} = 155$ V along with dc-link voltage. Fig. 8*a* shows the abovementioned parameters within one fundamental cycle while Fig. 8*b* demonstrates waveforms that correspond to several switching cycles. It should be noted that in the second case, the diode voltage V_{D01} is demonstrated instead of the dc-link and capacitor voltage. It can be seen that the voltage across the diode corresponds to the theoretical expectation; however, an high-frequency oscillation is also present. Middle point current may saturate the transformer core, which should be taken into consideration during the design of the transformer. Another solution is to use advanced modulation techniques with middle point current reduction.

It can be seen that our experimental results are very similar to the simulation results. The voltage spikes across semiconductors and the dc-link voltage are explained by the leakage inductance of the transformer. A more optimised design will significantly improve the situation. The measured efficiency of the experimental prototype was in the range 90–94%. The maximum efficiency corresponds to the VSI mode without the ST states and the modulation index is equal to 1. Introduction of the ST states will decrease the efficiency.

5 Conclusions

This paper has described and compared solutions for a family of new three-phase 3L NPC LCCT-derived inverters. Component design guidelines and steady state analysis, current and voltage waveforms are presented.

Our analysis has shown that the topologies with discontinuous input current contain the same amount and size of passive elements and offer no advantages over LCCT-derived inverters with CIC. Further, the CCM in the current inductor appeared insufficient to ensure normal operation of the proposed topologies. To provide converter performance in accordance with equivalent circuits, the capacitor current should not drop to zero during an active state. This condition should be taken into account in component design.

Our simulation results have confirmed all theoretical predictions. The main advantage of the proposed solutions over other IS-derived inverters lies in better dc-link utilisation along with the reduced capacitor size. It is of high significance for applications where high boost is required; semiconductors with lower voltage blocking capability for the same wide input voltage

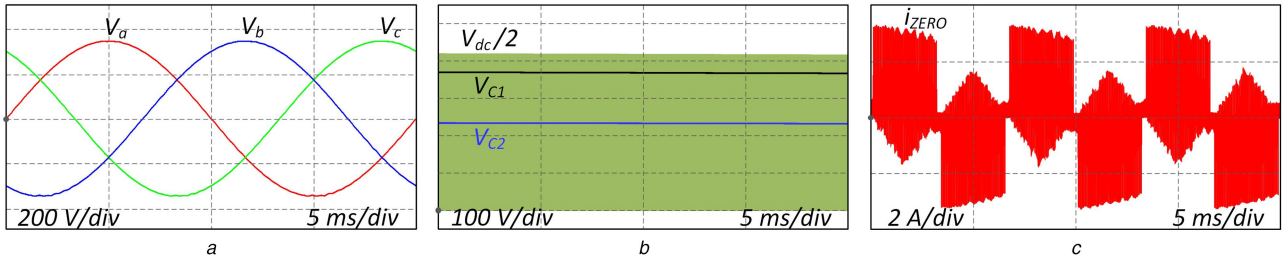

Fig. 5 *Simulation results of the separated 3L NPC LCCT Z-source network*
(a) Output voltage, ***(b)*** dc-link voltage, capacitor C_1–C_4 voltage, ***(c)*** Zero current

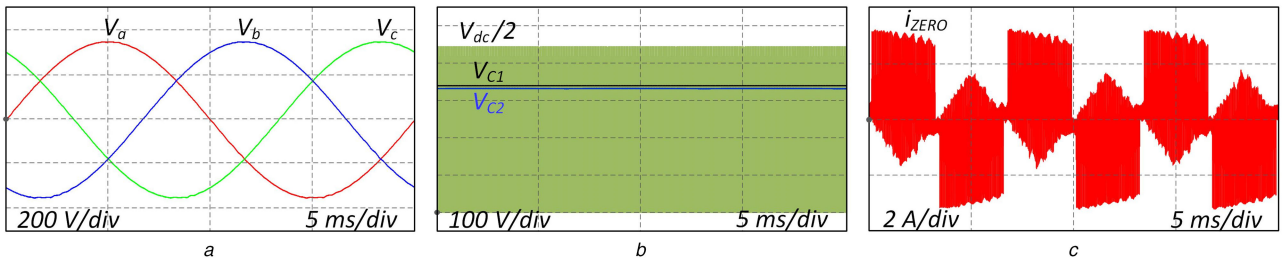

Fig. 6 *Simulation results of the 3L NPC LCCT Z-source network*
(a) Output voltage, ***(b)*** dc-link voltage, capacitor C_1–C_2 voltage, ***(c)*** Zero current

Table 3 System parameters used for experiments

Control unit (FPGA)	Cyclone IV EP4CE22E22C8
transistor driver chip	ACPL-H312
transistor T_1, …, T_{12}	C2M0080120
LCCT network and NPC diodes D_1, …, D_6	C3D10065A
D – ST duty cycle	0.2
n – inductor turns ratio	1.9
V_{IN} – input voltage	160 V
V_{OUT} – RMS output voltage	110 V
P – output power	300 W
T – switching cycle	10 µs
M – modulation index	0.8
C_1 – C_3 – capacitors	470 µF
L_1 – inductance	3.1 mH
L_{fa1}, L_{fb1}, L_{fc1} – first output filter inductors	0.5 mH
L_{fa2}, L_{fb2}, L_{fc2} – second output filter inductors	0.2 mH
C_{fa}, C_{fb}, C_{fc} – output filter capacitors	0.47 µF

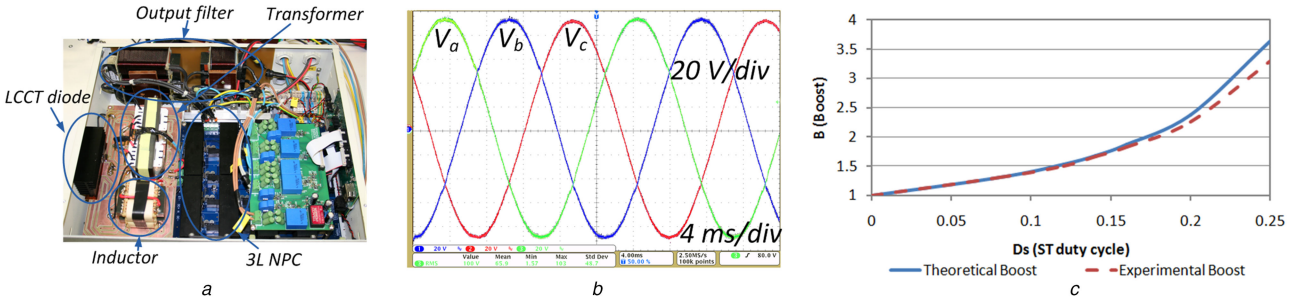

Fig. 7 *Experimental study of the 3L NPC LCCT Z-source network with a single input voltage source and CIC*
(a) Experimental setup, ***(b)*** Waveforms of the output voltage, ***(c)*** Comparison of the boost factors B obtained analytically (solid line) and experimentally (dashed line) versus the ST duty cycle

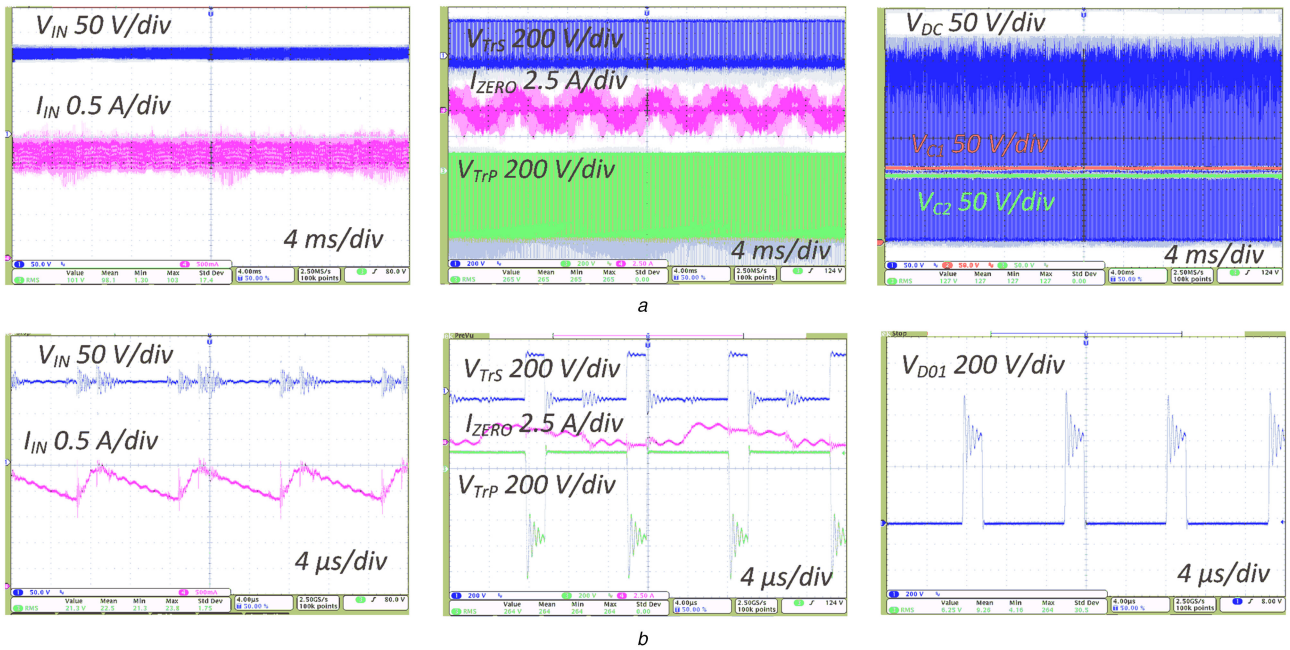

Fig. 8 *Experimental results of the 3L NPC LCCT Z-source network with a single input voltage source and CIC*
(a) Fundamental cycles, ***(b)*** Switching cycles

regulation range can be used. It is emphasised that the asymmetrical 3L NPC LCCT-derived inverter with a single input voltage source and CIC appears more attractive because of fewer passive components and one fewer diode in the IS network. Experimental results obtained for this topology proved all theoretical predictions.

In conclusion, the solution proposed can be applied at high boost with improved utilisation of the dc-link voltage. At the same time, attention should be paid to the magnetics design.

6 Acknowledgments

This research work was supported by Estonian Research Council grant no. PUT (PUT633), Latvian National Research Programme 'LATENERGI', Latvian Council of Science (grant no. 673/2014) and co-supported by Ukrainian Ministry of Education and Science (grant nos. 0116U004695 and 0116U006960).

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