

# Current Sensorless Control of Front-end Bidirectional AC/DC Converter Based on Half-bridge Topology

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**Abstract** – Electrical grid modernization concept promotes the use of DC subgrids in order to improve efficiency, minimizing energy conversion count in the source-to-load chain. The present paper discusses an average current sensorless control algorithm for proposed bidirectional AC/DC converter, which is based on a dual half-bridge topology with common neutral wire that is not commutating during converter operation. The proposed current sensorless control algorithm has been obtained analytically for rectification, grid-tied and stand-alone inverter modes. The average value of inductor current tracks the reference current signal with constant switching frequency. Two control functions for inductor's discontinuous and continuous current modes have been defined for each of the operation modes, and a sensorless transition between DCM and CCM modes has been stated. The proposed sensorless control algorithm has been also adapted for use with LCL input filter. The results of simulation in the PSIM software approved the analytical model, keeping the average inductor current to follow the reference value in inductor discontinuous and continuous conduction modes. Experimental investigation of the proposed current control algorithm provided similar results confirming the discussed theory.

**Keywords** – AC-DC power converters, sensorless control, current control, inverters, pulse width modulation converters.

## I. INTRODUCTION

The world's electrical energy demand is growing at a rate of 2.4% annually, while developing countries have 4% increase of demand [1] due to increasing population [2] and standards of living, forcing countries to install new generation facilities on a regular basis. While the consumption of fossil resources remains reasonable, countries invest finances into development of renewable energy sector. The total investment volume was estimated to be 257 billions of USA dollars in 2011 [3]. The result of these investments is a growing number of installed solar and wind energy capacities per annum, promoting significant reduction of technology costs. For instance, energy production cost in Germany is 0.138-0.163€/kWh for photo-voltaic (PV) plants [4].

Countries might also adapt their legislation concerning connection of small energy sources to the utility grids, so that the owners of the RES become prosumers (producer and consumer). Denmark shows a spectacular example of this approach, where 36 MW of PV panels are connected monthly to a grid in the residential sector, after it became allowed to "store" energy in public grid surplus consumption, thus helping to reach the 20-20-20 governmental goal of 200 MW PV capacity by the end of 2012 [5].

At the same time grid modernization concepts are developed, such as microgrid [6] and nanogrid [7], which are targeted for superior functionality of local grids with higher

efficiency and stability values. These concepts also promote the use of DC subgrids [8]–[10], which allows reducing energy conversion count, as a result reaching higher efficiency values [11]. The focus is on the bidirectional AC/DC converter, which is responsible for stability in both – AC and DC subgrids [12], or can be used to interface energy storage element [13]. In some cases AC/DC converter might also support AC grid by compensating higher harmonics [14].

This article is dedicated to the analysis of current sensorless control of the proposed bidirectional AC/DC converter based on half-bridge topology with common neutral point that is not commutating during the converter operation.

The article is structured as follows: firstly, the overview of sensorless control algorithms is discussed; then the proposed current sensorless control algorithm with constant switching frequency is developed for rectification, grid-tied and stand-alone inverter modes; afterwards, the calculation of LCL filter is made and adaptation of control algorithm is discussed; finally, the experimental results are presented and conclusions are drawn at the end of this paper.

## II. DESCRIPTION OF TOPOLOGY

Various bidirectional topologies are proposed for intelligent grid applications, for instance: non-isolated converter with half-bridge that interfaces AC side and full-bridge interfacing DC side [15], DAB topology with non-resonant [16] or resonant [17] isolation stage. The first one is not safe, because both terminals of DC grid are under high potentials, while two other are bulky due to the use of transformer.

Hereby, the authors would like to propose bidirectional interface converter with common neutral, which is not commutating during converter's operation that provides safe utilization. Besides the half-bridge topology is preferable due to minimized semiconductor switch count in the current path [18], where the problem of transistor's overvoltage can be solved with proper design as discussed in [19]. The DC side mostly charges and discharges the capacitor C1, a balancing circuit is utilised, but not analysed in the present paper.

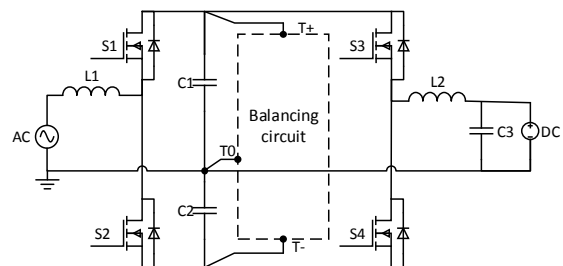


Fig. 1. Proposed bi-directional AC/DC converter's topology.

### III. CURRENT CONTROL

Multiple current control techniques are known from the literature [20]–[23]: peak current control, hysteresis, delta modulation, boundary switching, which relate to current measurement and all are relevant in some specific applications. On the other hand, input inductor current sensing in high frequency switched mode power supplies (SMPS) is the most challenging task, which also significantly increases the cost and size of control system as it was mentioned in various articles [24]–[26], while the importance of the fast current loop has been discussed in [27]. The current sensorless control techniques are then proposed. They eliminate instantaneous current measurement, but use other approaches for estimation of input current. In [28] it is proposed to use a slower load current measurement to estimate current of input inductor. It is advised by the authors from [29] to use an average inductor current sensor that is suitable for digital control systems. In [30] the single-loop current sensorless control is being proposed, which is based on digital current rebuilding approach and uses input and output voltage values as well as predefined circuit parameters (inductor and capacitor precise values) to estimate instantaneous inductor current value. The fixed and variable switching frequencies are used in the above mentioned articles, however, according to [31], the constant frequency reduces switching losses in comparison with variable frequency control, as well as reduces high-frequency components.

The comparison with other sensorless control approaches is provided in Table I.

TABLE I  
OVERVIEW OF DIFFERENT SENSORLESS CONTROL TECHNIQUES

	[30]	[32]	[33]	[34]	Proposed
Fixed switching frequency	✓	✓	✓	✓	✓
Fixed-amplitude carrier	✓	✓			✓
Current form	DCM				✓
	CCM	✓	✓	✓	✓
Stable to non-sinusoidal input voltage		✓		✓	✓
Current sensorless	✓	✓			✓
Input voltage sensorless			✓	✓	

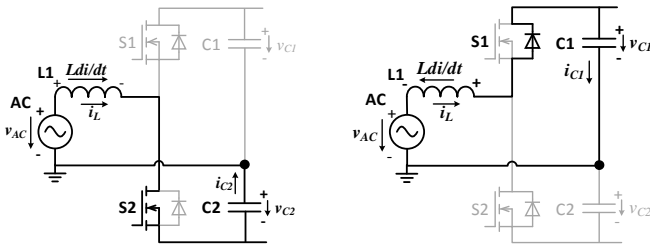


Fig. 2. Commutated current paths in rectification mode during positive half-period of input voltage.

#### A. Rectifier mode

The typical operation of half-bridge topology in active rectifier mode is shown in the figure above (see Fig. 2) (the positive half period is considered). The current forms during one switching period are seen in the figure below.

Assuming that capacitor voltages remain constant during one switching period, but input voltage is averaged, inductor's maximal current (Fig. 3) is described by voltage applied to inductor  $L$  during transistor's conduction time ( $t_{1,k}$ ) and diode's conduction time ( $t_{2,k}-t_{1,k}$ ) as:

$$i_{\max,k} = \frac{v_{C2,k} + v_{AC\_avg,k}}{L} \cdot t_{1,k} \quad \text{and} \quad (1)$$

$$-i_{\max,k} = \frac{v_{C1,k} - v_{AC\_avg,k}}{L} \cdot (t_{2,k} - t_{1,k}). \quad (2)$$

where  $L$  is input inductor inductance,  $V_{C1}$  and  $V_{C2}$  are capacitors' voltages,  $V_{AC\_avg}$  is input sinusoidal voltage averaged during one switching period, but index  $k$  indicates discrete values during  $k^{\text{th}}$  switching period.

The average inductor current ( $i_{avg,k}$ ) during one switching period ( $T_{sw}$ ) is defined as:

$$i_{avg,k} = \frac{i_{\max,k} \cdot t_{2,k}}{2 \cdot T_{sw}}. \quad (3)$$

Taking into account equations (1)–(3) the transistor conduction time during DCM mode is defined as:

$$t_{1,k} = \sqrt{\frac{|i_{avg,k}| \cdot 2 \cdot L \cdot T_{sw} \cdot (v_{C1,k} - v_{AC\_avg,k})}{(v_{C2,k} + v_{AC\_avg,k}) \cdot (v_{C1,k} + v_{C2,k})}}. \quad (4)$$

During CCM period another control law should be used, taking into account that  $t_{2,k}$  now is equal to switching period  $T_{sw}$ . Transistor conduction time can be extracted from equation below:

$$\frac{v_{C2,k} + v_{AC\_avg,k}}{L} \cdot t_{1,k} + \frac{v_{C1,k} - v_{AC\_avg,k}}{L} (T_{sw} - t_{1,k}) = \Delta i_{ref,k}, \quad (5)$$

which can be explained as integral of voltage applied to inductor during one switching period that is equal to reference current discrete change during one switching period ( $\Delta i_{ref}$ ). So that the control law for CCM period is defined as:

$$t_{1,k} = \frac{\Delta i_{ref,k} \cdot L + (v_{C1,k} - v_{AC\_avg,k}) \cdot T_{sw}}{(v_{C1,k} + v_{C2,k})}. \quad (6)$$

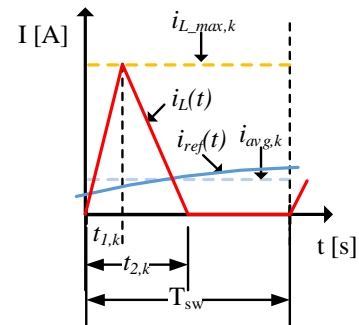


Fig. 3. Inductor's current form during single switching period in DCM.

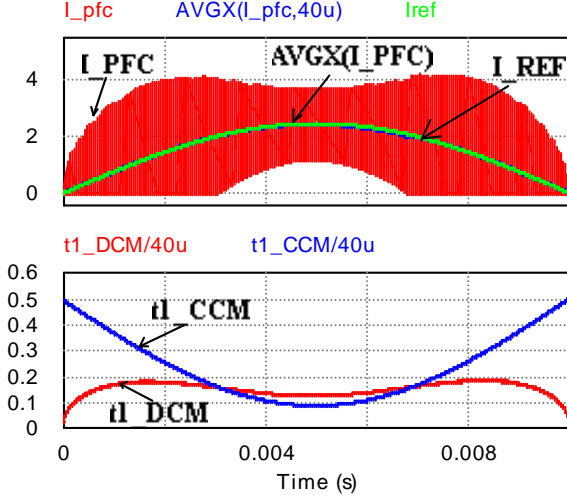


Fig. 4. Simulation result for rectification mode (amplitude of reference current signal  $I_M = -2.5$  A).

The simulation in PSIM software was made in order to evaluate obtained control laws. The figure above demonstrates two graphs with current forms (top graph) and both control laws (bottom graph). Inductor's  $L1$  current (red) is seen in the upper graph of Fig. 4, the average current (blue) of which is following reference current form (green). The lower graph represents DCM and CCM timing functions, which cross at boundary conduction mode. The control system chooses minimal value between (4) and (6) to control the transistor.

### B. Grid-tied inverter mode

The commutated current paths of half-bridge interface converter in grid-tied inverter mode are presented in Fig. 5 (positive half-period of input voltage is considered).

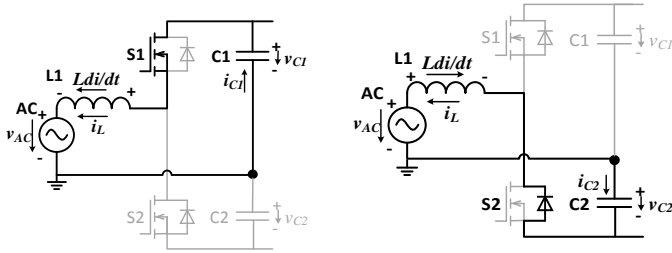


Fig. 5. Commutated current paths in grid-tied inverter mode during positive half-period of input voltage.

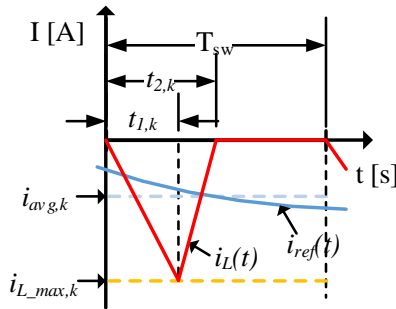


Fig. 6. Inductor current form in grid-tied inverter mode during one switching period.

The grid-tied inverter mode is analysed similarly to rectification one, concerning that S1 transistor is commutating during positive half period of input voltage (Fig. 6).

Thus, the control law for DCM is defined as:

$$t_{1,k} = \sqrt{\frac{|i_{av,g,k}| \cdot 2 \cdot L \cdot T_{sw} \cdot (v_{C2,k} + v_{AC\_avg,k})}{(v_{C1,k} - v_{AC\_avg,k}) \cdot (v_{C1,k} + v_{C2,k})}}, \quad (7)$$

while inductor current in CCM is controlled by using the following definition, which is obtained in the same way as in (6):

$$t_{1,k} = \frac{-\Delta i_{ref,k} \cdot L + (v_{C2,k} + v_{AC\_avg,k}) \cdot T_{sw}}{(v_{C1,k} + v_{C2,k})}. \quad (8)$$

The results of simulation of operation of half-bridge converter in grid-tied inverter mode are presented below (Fig. 7). The upper graph demonstrates the current flow in input inductor, which is similar to current form simulated for rectifier mode. The lower graph presents the transistor S1 conduction time, where two functions (DCM and CCM control laws) are crossing at boundary conduction mode.

### C. Stand-alone inverter mode

The stand-alone inverter mode (Fig. 8) requires different control law than in grid-connected mode, as capacitor voltage on one side and voltage drop across the load from other side are balanced with electromotive force of input inductor. As a result inductor  $L1$  current is changing in an exponential way.

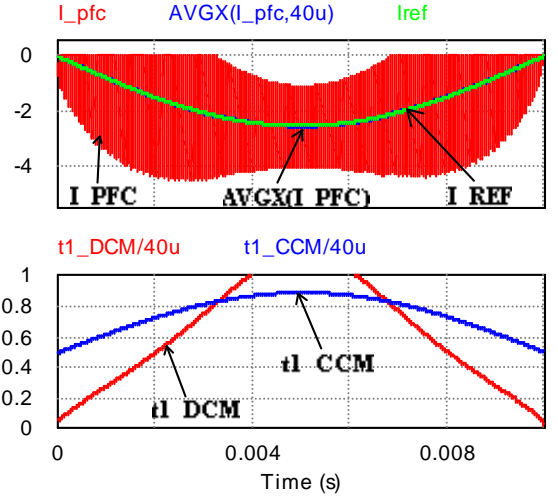


Fig. 7. Simulation result for grid-tied inverter mode ( $I_M = -2.5$  A).

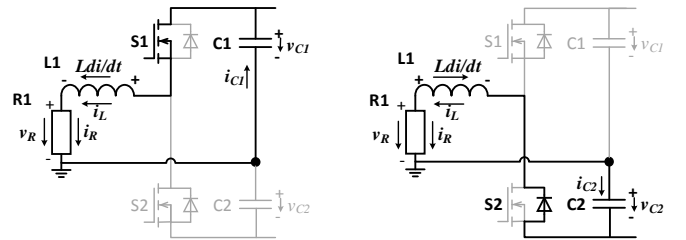


Fig. 8. Commutated current paths in stand-alone inverter mode during positive half-period of generated voltage.

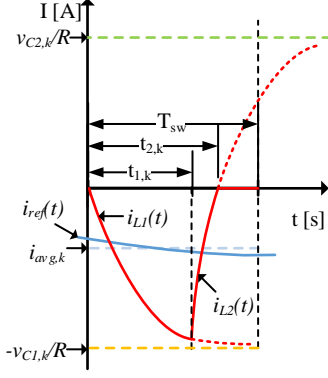


Fig. 9. Inductor current form in stand-alone inverter mode during one switching period.

Two equations below ((9) and (10)) describe the rising and falling current forms (Fig. 9):

$$i_L(t) = \int_{t_{0,k}}^{t_{1,k}} (-v_{C1}(t) - R \cdot i_L(t)) dt, t \in [t_{0,k}, t_{1,k}] \text{ and} \quad (9)$$

$$i_L(t) = \int_{t_{1,k}}^{t_{2,k}} (v_{C2}(t) - R \cdot i_L(t)) dt + i_L(t_{1,k}), t \in [t_{1,k}, t_{2,k}], \quad (10)$$

where  $R$  is load resistance.

By solving above differential equations, the following results are obtained:

$$i_L(t) = -\frac{v_{C1,k}}{R} \cdot \left(1 - e^{-\frac{R}{L}t}\right), t \in [t_{0,k}, t_{1,k}] \text{ and} \quad (11)$$

$$i_L(t) = \frac{v_{C2,k}}{R} \cdot \left(1 - e^{-\frac{R}{L}(t-t_2)}\right), t \in [t_{1,k}, t_{2,k}]. \quad (12)$$

The  $t_{2,k}$  timing function can be defined from (9) and (10) as follows:

$$t_{2,k} = -\frac{(v_{C1,k} + v_{C2,k}) \cdot t_{1,k} + R \cdot i_{avg,k} \cdot T_{sw}}{v_{C2,k}}. \quad (13)$$

In order to obtain control law for stand-alone inverter mode, the (11) and (12) are equalized at time  $t_{1,k}$ . After rearranging variables the equation looks like:

$$\frac{v_{C2,k}}{v_{C1,k}} e^{-\frac{R}{L}t_{1,k}} = \left(1 - \frac{v_{C2,k}}{v_{C1,k}}\right) e^{-\frac{R}{L}t_{2,k}} - e^{-\frac{R}{L}(t_{1,k}+t_{2,k})}, \quad (14)$$

that makes sense of transcendental equation, as trying to extract natural logarithms from both parts, the timing function  $t_{1,k}$  will be defined by natural logarithm that contains the same timing function. Thus, this equation has no algebraic solution, however, it could be simplified assuming that the ratio of voltages are approximately equal to 1, and, secondly, the last part has the smallest contribution to all the equation, because of largest absolute value of exponent, which due to negative sign tends to zero faster than other parts containing exponent. Thus, the result of simplification is written as:

$$e^{-\frac{R}{L}t_{1,k}} = 2e^{-\frac{R}{L}t_{2,k}}, \quad (15)$$

which in contrast to (14) has an algebraic solution. Taking into account  $t_{2,k}$  definition from (13), the control law is defined as:

$$t_{1,k} = \frac{R \cdot i_{avg,k} \cdot T_{sw}}{v_{C1,k}} - \frac{v_{C2,k} \cdot L}{v_{C1,k} \cdot R} \cdot \ln \frac{1}{2}. \quad (16)$$

The simplified control law is admissible at more or less equal capacitor voltages and relatively high resistance of the load, while precise control law can be obtained only by using numerical methods for solving transcendental equations, for example, bisection method. The figure below demonstrates graphical representations of simplified and precise control laws for different amplitudes of reference signal. The two curves are almost identical at light loads (Fig. 10 (a)), while the difference is more noticeable at higher loads (Fig. 10 (b)).

The control law for CCM is defined similarly as it was done previously for rectification or grid-tied inverter mode, resulting in:

$$t_{1,k} = \frac{-\Delta i_{ref,k} \cdot L + (v_{C2,k} + R \cdot i_{ref-avg}) \cdot T_{sw}}{(v_{C1,k} + v_{C2,k})}. \quad (17)$$

In order to verify obtained control laws for stand-alone inverter mode, the simulation in PSIM was made, where bisection method was implemented to obtain the transistor's conduction time during DCM (Fig. 11).

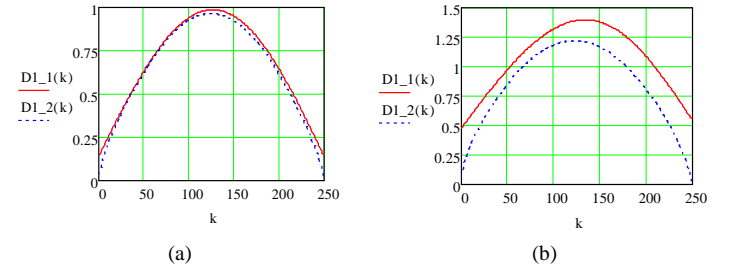


Fig. 10. Graphical representation of simplified (D1\_1) and precise (D1\_2) control laws for stand-alone inverter mode: (a)  $I_M = -2.5$  A,  $R = 124.4$  Ω; (b)  $I_M = -8.5$  A,  $R = 36.6$  Ω; (index  $k$  identifies sequential number of switching period, where 250 switching periods correspond to half-period of 50 Hz sinusoidal signal operating at 25 kHz).

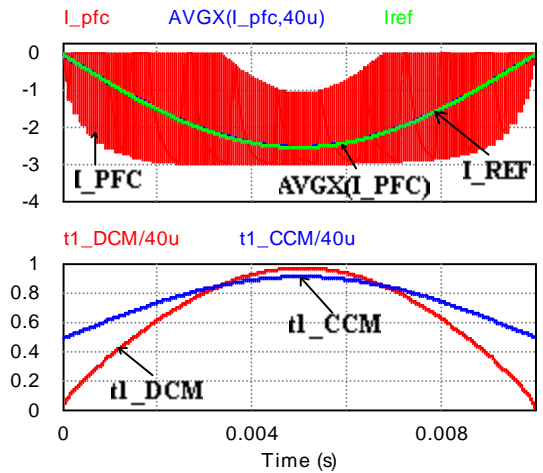


Fig. 11. Simulation result for stand-alone inverter mode ( $I_M = -2.5$  A,  $R = 124.4$  Ω).

#### IV. LCL FILTER

As it was previously observed from simulations, the current consumed or generated into the grid hardly remind the sinusoid, because of high amount of higher harmonics located close to the converter's switching frequency. The LCL filter (see Fig. 8) is commonly used for reduction of harmonics as described in [35] and [36], that requires special care of calculation keeping trade-off between quality of input current and dimensions of the filter, which are also proportional to filter's price.

##### A. Calculation

The converter-side inductor is selected by using boost converter's inductance selection equation, where current ripple is limited by capacitor's admissible ripple value. The ALC10A471DF450 capacitor is considered to be used in AC/DC converter with 4.03 A of admissible current ripple [37]

$$L_{F2} = \frac{(v_{C2,k} + v_{AC,k}) \cdot D_k}{f_{SW} \cdot \Delta I_{ripple}}. \quad (18)$$

The filter capacitor is selected in order to shunt higher harmonic currents with the capacitor branch, selecting impedance of the capacitor lower than grid-side inductor's impedance (about 1/10 or 1/5 of  $X_{L_G}$ ):

$$X_{CF} = \left( \frac{1}{10} \text{ to } \frac{1}{5} \right) X_{L1}. \quad (19)$$

If the constraint is not fulfilled and capacitor impedance is comparable with grid side inductor's impedance, the filter capacitor will not be able to shunt enough the current ripple and more distorted current will be injected into the grid. On the other hand – larger capacitance will result in the increased reactive power flow. The reactive power limit is usually selected below 5% of system rated power [38]. Thus, the capacitance limit is defined as:

$$C_F \leq 0.05 \frac{P}{2\pi \cdot f_{AC} \cdot V_{AC}^2}, \quad (20)$$

where  $V_{AC}$  is RMS value of input voltage,  $P$  is rated power,  $f_{AC}$  grid's frequency. The  $C_F$  value of 1.6  $\mu F$  is selected for 1 kW converter, which corresponds to 2.5% of rated converter's base impedance.

Another constraint is related with LCL filter self-resonance frequency, which is defined by the following equation:

$$f_{res} = \frac{1}{2\pi} \sqrt{\frac{L_{F1} + L_{F2}}{L_{F1} \cdot L_{F2} \cdot C_F}}. \quad (21)$$

The resonant frequency should match the following constraint:

$$10f_{AC} < f_{res} < \frac{1}{2} f_{SW}. \quad (22)$$

Selecting 0.2 mH for grid-side inductor both constraints ((19) and (20)) are fitted, as grid-side inductor's impedance is tenfold in comparison with selected filter capacitor impedance and LCL filter's resonance frequency (6 kHz) is located within the defined range ( $10 \cdot 50 \text{ Hz} < f_{res} < 25/2 \text{ kHz}$ ).

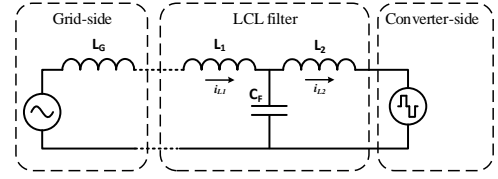


Fig. 12. Location of LCL filter.

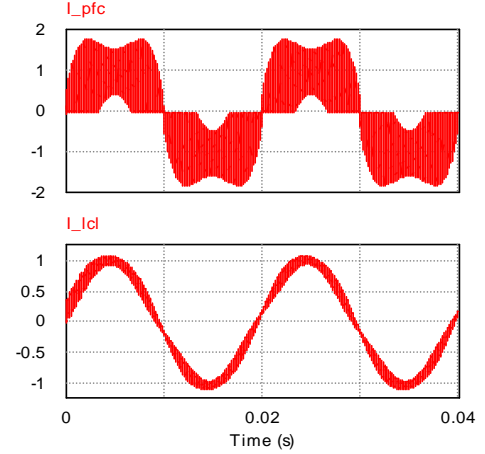


Fig. 13. Simulation results for evaluation of LCL filter.

TABLE I  
PERFORMANCE OF LCL FILTER

	$I_M$ [A]	7.5	5	2.5	1	0.5
Rectifier mode	THD( $I_{L2}$ )[%]	13.6	19.5	34.9	67.3	101.2
	THD( $I_{L1}$ )[%]	1.8	2.7	4.5	8.2	11.5
Inverter mode	THD( $I_{L2}$ )[%]	12.1	17.7	32.4	63.8	96.1
	THD( $I_{L1}$ )[%]	1.7	2.5	4.4	8.2	11.5

The figure below demonstrates the performance of LCL filter, where the top graph represents converter-side inductor's current, while bottom graph corresponds to grid-side inductor current.

The following table contains converter-side and grid-side inductors currents THD values obtained by simulation in PSIM at different input current reference values.

##### B. Adaptation of proposed switching technique

Special consideration should be taken into account in order to use previously obtained control laws for converter operation with LCL filter. During DCM mode only converter-side inductor should be taken into account to calculate the transistor's duty cycle for rectification and grid-tied inverter modes. During CCM the total inductance of the LCL filter should be considered to calculate transistor's conduction time for rectification and grid-tied inverter modes.

The stand-alone inverter's mode with LCL filter should be treated as grid-tied inverter mode as the current waveforms are not exponential, but linear due to filter capacitor.

## V. EXPERIMENTAL INVESTIGATION

The performance of the elaborated bidirectional AC/DC converter was tested at a reduced input voltage to evaluate the proposed current sensorless control algorithm driven by FPGA control board.

The figure below (see Fig. 15.) demonstrates the transition between disabled PFC function and enabled PFC function. As it can be noted, the current shape was with improved  $PF > 0.97$ , and THD value (around 10%), that was relatively good result, due to the fact that CCM period constituted 70% of sinusoidal half-period.

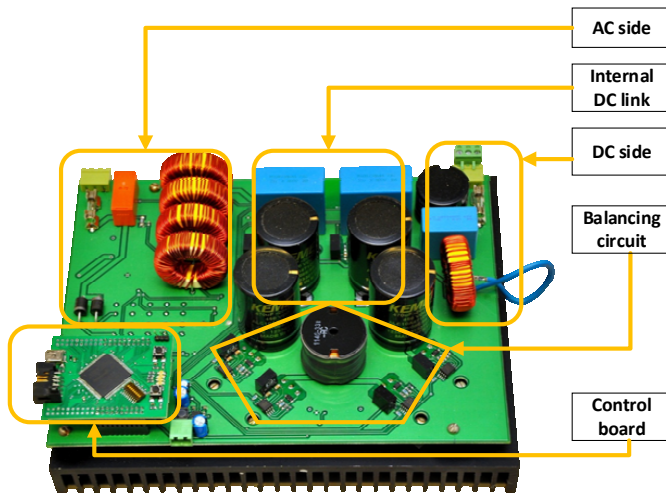


Fig. 14. Photo of bidirectional AC/DC converter.

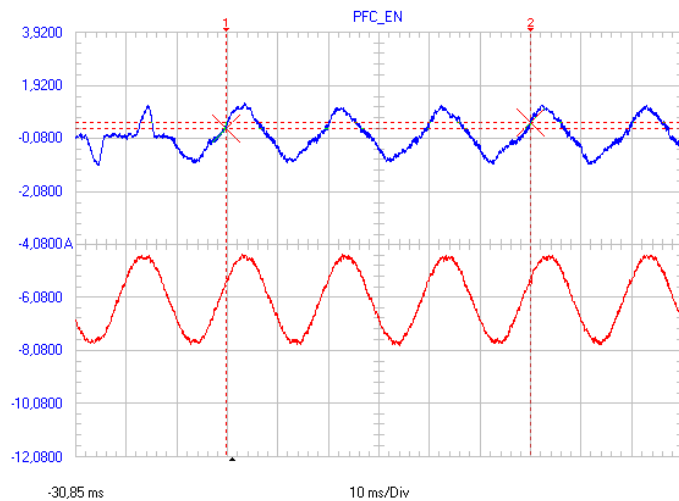


Fig. 15. Performance of the PFC function - current (blue, 2 A/div) and input voltage (red, 100 V/div).

## VI. CONCLUSIONS

The proposed bidirectional AC/DC dual half-bridge converter has advantage over other solutions due to non-commutating neutral wire that eliminates also the use of transformer; thus, the power density of the converter can potentially be increased. The current sensorless control algorithm has lower cost and size of the control system in comparison with sensed control. Proposed algorithm has been obtained analytically and confirmed by simulations for all operation modes. The constant switching frequency potentially allows keeping the high performance of the LCL filter at wide range of power ratings.

Proposed average current sensorless control algorithm can be also applied in sensed applications during low power modes, where inductor's current is mostly discontinuous and there is certain difficulty to sample current during small duty cycle. Thus, the current shape can be improved by utilising proposed technique, which allows calculating the duty cycle with high precision.

The experimental investigation of proposed converter was performed at reduced input voltage ratings, where it was noticed relatively high THD value of inductor current. It could be explained with imprecision of calibration of analogue to digital converter, as well as parasitic voltage drops on semiconductor and reactive elements, causing deviation in voltage-second balance on inductor, which resulted in distortion of sinusoidal current form. Thus, proposed current control algorithm can be improved further taking into account the mentioned problems.

## ACKNOWLEDGEMENTS

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