

# Improved Switched-Inductor Quasi-Switched-Boost Inverter with Low Input Current Ripple

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**Abstract** – The quasi-switched-boost inverter is an alternative to the quasi-Z-source inverter. Its passive component number is two times smaller but it contains two additional semiconductor components. Earlier the switched-inductor cell was applied in this topology to enhance dc voltage gain at the cost of high input current ripple. This paper proposes a novel switched-inductor quasi-switched-boost inverter topology with low input current ripple and enhanced dc voltage gain. It is based on a modified switched-inductor cell where the input source is connected in series with an inductor. Operation principle is described through separation of the switching period into three intervals. Equivalent circuits and circuit equations are shown for each interval. Simulation study corroborates theoretical predictions.

**Keywords** – dc-ac converter, inverter, impedance-source inverter, switched-boost inverter, switched-inductor.

## I. INTRODUCTION

Impedance-source (IS) converters are an emerging technology of single-stage buck-boost electric energy conversion for applications with wide input voltage variations [1]. This field of research was initiated in 2003 after Z-source inverter (ZSI) was proposed in [2]. The IS technology was applied to dc-dc and ac-ac converters, inverters, circuit breakers to overcome limitations of conventional solutions [1],[3],[4]. Hence, application range of the IS technology is wide, while most of the studies show their superior performance in renewable and alternative energy, and motor applications. The quasi-Z-source inverter (qZSI) was derived from ZSI by position rearrangement of the input source to achieve continuous input current and lower voltage stress, while saving all advantages of the ZSI [5],[6]. Since then the ZSI and the qZSI are usually considered as reference topologies of IS inverter. They provide buck-boost operation by controlling the modulation index in the buck mode and the shoot-through state duration in the boost mode. However, the relatively high number of passive components can cause a small efficiency drop as compared to conventional solutions.

The switched-boost inverter (SBI) was proposed in [7] as a simpler alternative to the ZSI that contains only a single capacitor and a single inductor. This is half as many passive components as in the ZSI. The SBI features discontinuous input current and lower dc voltage gain than that of the ZSI/qZSI. Moreover, it requires an additional diode and an auxiliary switch. The quasi-switched-boost inverter (qSBI) shown in Fig. 1 is an improved derivative of the SBI and thus contains the same number of components. It was first proposed in [8] and recently extended to a family of the qSBI

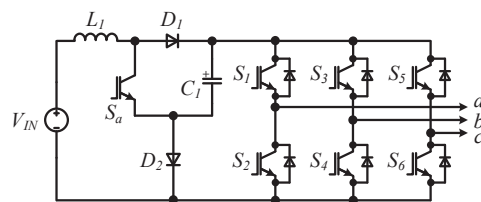


Fig. 1. Quasi-switched-boost inverter (qSBI) topology [8], [9].

topologies in [9]. As distinct from the SBI, the qSBI provides continuous input current and the same dc voltage gain as the qZSI. In practice the qSBI can outperform the qZSI by voltage step-up due to a lower number of passive components, which results in lower parasitic losses within them [10].

In emerging energy applications with wide voltage variations, like solar photovoltaic and wind energy, non-isolated inverters with high dc voltage gain are required for grid integration. They allow utilization of low voltage/energy levels and thus maximize energy yield in unfavorable climatic conditions. The qSBI seems an attractive topology that could overcome limitations of the qZSI, while its dc voltage gain is rather moderate and thus has to be improved.

Dc voltage gain can be improved using one of three major techniques, which were applied to IS inverters recently. First, IS network can be cascaded to enhance dc voltage gain, like in extended boost cascaded qZSI [11]. However, this method requires additional passive components. Second, coupled inductors can be used to derive a new IS network with higher dc voltage gain [12]-[16]. However, most of them suffer from duty cycle loss caused by leakage inductance of a coupled inductor [17]. Third, switched-inductor and switched-capacitor cells proposed in [18], as well as other voltage lift cells derived from them [15], [19], can be applied to most of the IS networks. Hence, it has been applied to the ZSI [20]-[23], the qZSI [24]-[27] and other inverters. The switched-inductor cell (SL) is used most extensively for dc voltage gain enhancement.

The SL cell was applied to SBI in [28] to enhance its dc voltage gain. The qSBI has also benefited from the utilization of the SL. The switched-inductor qSBI (SL-qSBI) presented in [29] has improved the dc voltage gain characteristic, while the input current ripple is much higher than that in the qSBI. The input current ripple of the SL-qSBI (Fig. 2a) is equal to the average current of the SL inductors  $L_1$ ,  $L_2$  (Fig. 2b).

This paper presents an improved SL-qSBI with low input current ripple (cSL-qSBI). It is derived from the SL-qSBI by moving of the input source to connect it in series with one of

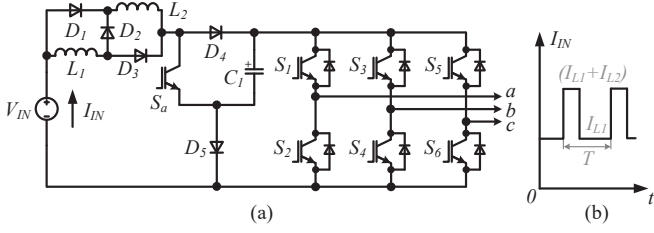


Fig. 2. The SL-qSBI topology [29] (a) and sketch of its input current (b).

inductors of the SL. A similar approach was used in [22], [26] to improve switched-inductor based ZSI and qZSI. It results in considerable reduction of the input current ripple. Moreover, this paper describes differences in the current ripple of the SL inductors, which was not shown in [22] and [26]. Different voltages applied to these inductors during shoot-through state result in different current ripple and dividing of the conventional active state into two different sub-intervals.

## II. DERIVATION AND OPERATION PRINCIPLE OF IMPROVED SWITCHED-INDUCTOR QSBI

### A. Derivation of the cSL-qSBI

A sketch of input current ripple of the SL-qSBI is shown in Fig. 2b. The current ripple is considerably higher than that of the qSBI, while the current ripple of the inductors of SL is much lower. Hence, the input source can be connected in series with one of them to decrease the input current ripple, as shown in Fig. 3. The cSL-qSBI proposed contains the same amount of components as the SL-qSBI: five diodes  $D_1 \dots D_5$ , a single auxiliary switch  $S_a$ , a single capacitor  $C_1$ , two inductors  $L_1$  and  $L_2$ , and the three-phase voltage-source inverter  $S_1 \dots S_6$ .

### B. Operation Principle of the cSL-qSBI

Operation principle of the cSL-qSBI can be described using a simplified circuit shown in Fig. 4. The resistance  $R_{ld}$  is representing a load of the inverters. It is assumed to be constant since the dynamics of the inverter is relatively slow and there is an insignificant change of the load current during a single switching period  $T$ . The switch  $S_{pn}$  is used to imitate

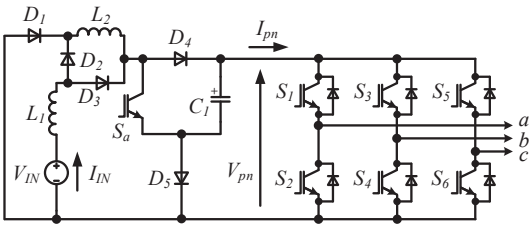


Fig. 3. Proposed cSL-qSBI topology that features low input current ripple.

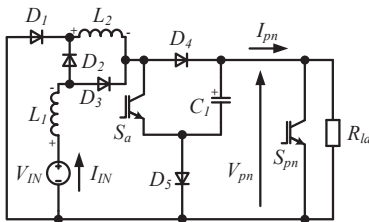


Fig. 4. Simplified circuit of the cSL-qSBI.

the shoot-through state. It is controlled synchronously with the auxiliary switch  $S_a$  – they both are turned on during the shoot-through state. For simplicity it is assumed that  $L_1 = L_2 = L$ .

Idealized voltage and current waveforms that describe the operation principle of the lossless converter are shown in Fig. 5. It is evident that currents of the SL inductors differ as they operate with different voltages. Both switches are controlled using the same switching sequence. Since the SL inductors operate asymmetrically, certain time is required to equalize this current at the beginning of the active state.

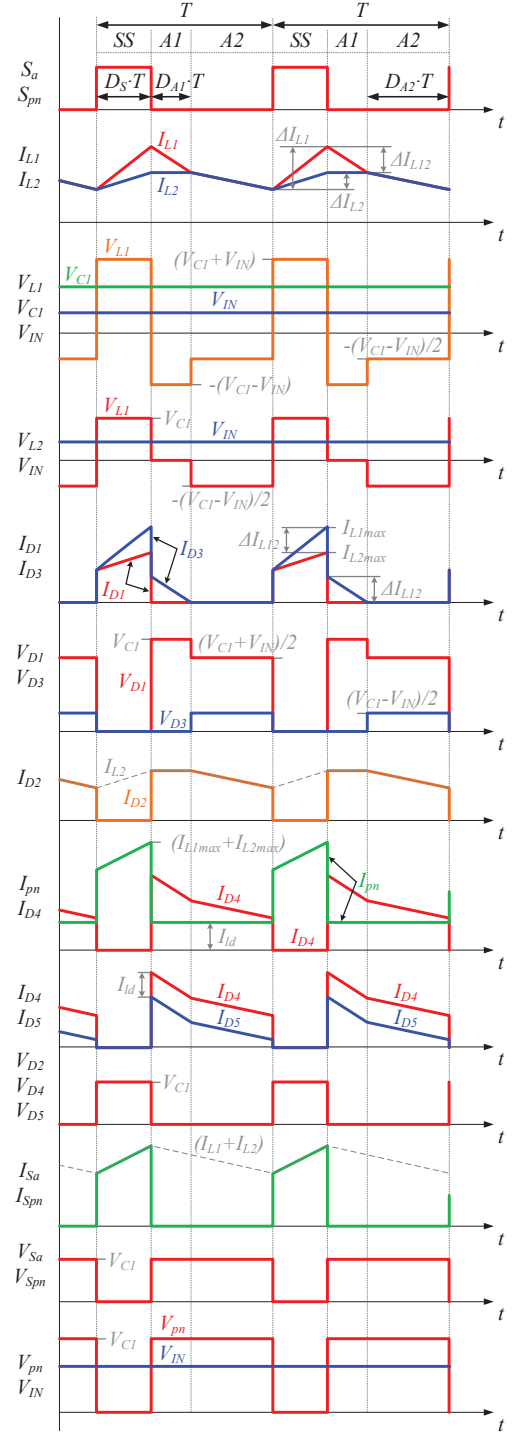


Fig. 5. Idealized current and voltage waveforms of the cSL-qSBI.

Consequently, the cSL-qSBI features two different active states. Hence, the switching period can be divided into three time intervals.

1) **SS** – the converter is in the shoot-through state. Equivalent circuit for this state is shown in Fig. 6a. Both switches are turned on. The output of the active IS network is short-circuited with the switch  $S_{pn}$ . The input source  $V_{IN}$  and the capacitor  $C_1$  are charging inductors  $L_1$ ,  $L_2$ , and thus their currents are rising. Meanwhile, their rates of rise are different due to reduced voltage applied to the inductor  $L_2$ , as compared to the conventional SL-qSBI [29]. Hence, the current  $I_{L1}$  reaches higher value than the current  $I_{L2}$ , considering that  $L_1 = L_2$ . The capacitor  $C_1$  is discharging with current  $(I_{L1} + I_{L2})$  during this interval. The SL inductors accumulate energy to be released during the active state. The duration of this interval is  $D_S \cdot T$ , where  $D_S$  is the shoot-through duty cycle. The following equations are describing the shoot-through state:

$$V_{L1} = L \frac{dI_{L1}}{dt} = V_{C1} + V_{IN}, \quad (1)$$

$$V_{L2} = L \frac{dI_{L2}}{dt} = V_{C1}, \quad (2)$$

$$V_{pn} = V_{Sa} = 0, \quad (3)$$

$$I_{Sa} = I_{pn} = -I_{C1} = I_{L1} + I_{L2}, \quad (4)$$

$$V_{D1} = V_{D3} = 0, \quad (5)$$

$$V_{D2} = V_{D4} = V_{D5} = V_{C1}, \quad (6)$$

$$I_{D1} = I_{L2}, \quad (7)$$

$$I_{D3} = I_{L1}, \quad (8)$$

$$I_{D2} = I_{D4} = I_{D5} = 0, \quad (9)$$

$$\Delta I_{L1} = \frac{V_{C1} + V_{IN}}{L} \cdot D_S \cdot T, \quad (10)$$

$$\Delta I_{L2} = \frac{V_{C1}}{L} \cdot D_S \cdot T, \quad (11)$$

$$\Delta I_{L12} = \frac{V_{IN}}{L} \cdot D_S \cdot T. \quad (12)$$

2) **A1** – the converter is in the first active state. During this time interval the SL inductors release energy to the load. The load is simulated with current  $I_{ld} = V_{C1}/R_{ld}$ . An equivalent circuit for this state is shown in Fig. 6b. A process of current equalizing of the SL inductors defines this interval, which ends when currents of the SL inductors are equal. This type of active state is obvious in the modified SL used here and in [22], [26]. However, this behavior has not been reported anywhere before. The diode  $D_3$  is conducting the surplus current  $(I_{L1} - I_{L2})$ . Hence, zero voltage is applied to the inductor  $L_2$  and thus its current  $I_{L2}$  is constant, while the current  $I_{L1}$  is decreasing. The SL supplies the load current and charges the capacitor  $C_1$  simultaneously. The duration of this interval is  $D_{A1} \cdot T$ . The following equations describe the first active state:

$$V_{L1} = L \frac{dI_{L1}}{dt} = -(V_{C1} - V_{IN}), \quad (13)$$

$$V_{L2} = L \frac{dI_{L2}}{dt} = 0, \quad (14)$$

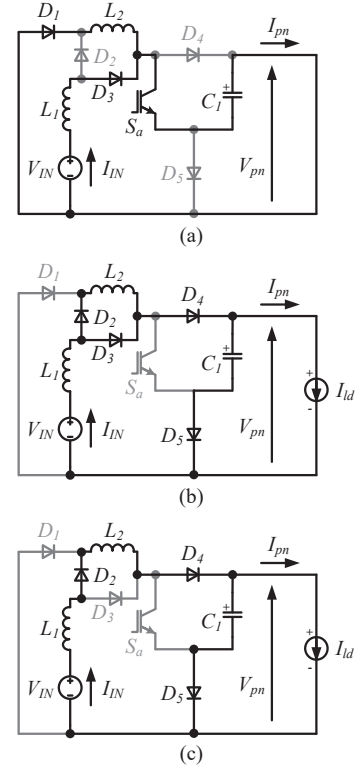


Fig. 6. Equivalent circuits of the proposed cSL-qSBI topology for: (a) shoot-through state SS, (b) first active state A1, and (c) second active state A2.

$$V_{pn} = V_{Sa} = V_{C1}, \quad (15)$$

$$I_{Sa} = 0, \quad (16)$$

$$I_{pn} = I_{ld} = \frac{V_{C1}}{R_{ld}}, \quad (17)$$

$$V_{D1} = V_{C1}, \quad (18)$$

$$V_{D2} = V_{D3} = V_{D4} = V_{D5} = 0, \quad (19)$$

$$I_{D1} = 0, \quad (20)$$

$$I_{D2} = I_{L2}, \quad (21)$$

$$I_{D3} = I_{L1} - I_{L2}, \quad (22)$$

$$I_{D4} = I_{L1}, \quad (23)$$

$$I_{D5} = I_{C1} = I_{L1} - I_{ld}. \quad (24)$$

3) **A2** – the converter is in the second, conventional, active state. During that time interval the SL inductors continue releasing energy to the load. Equivalent circuit for this state is shown in Fig. 6c. This interval ends at the end of the period, i. e.  $D_{A2} = (1 - D_S - D_{A1})$ . The diode  $D_3$  stops conducting because the currents of the SL inductors are equal:  $I_{L1} = I_{L2}$ . These currents are decreasing with the same slope. The SL continues supplying the load current and charging the capacitor  $C_1$  simultaneously. The following equations are describing the second active state:

$$V_{L1} = V_{L2} = L \frac{dI_{L1}}{dt} = L \frac{dI_{L2}}{dt} = -\frac{(V_{C1} - V_{IN})}{2}, \quad (25)$$

$$V_{pn} = V_{Sa} = V_{C1}, \quad (26)$$

$$I_{Sa} = 0, \quad (27)$$

$$I_{pm} = I_{ld} = \frac{V_{C1}}{R_{ld}}, \quad (28)$$

$$I_{L1} = I_{L2}, \quad (29)$$

$$V_{D1} = \frac{V_{C1} + V_{IN}}{2}, \quad (30)$$

$$V_{D3} = \frac{V_{C1} - V_{IN}}{2}, \quad (31)$$

$$V_{D2} = V_{D4} = V_{D5} = 0, \quad (32)$$

$$I_{D1} = I_{D3} = 0, \quad (33)$$

$$I_{D2} = I_{D4} = I_{L1} = I_{L2}, \quad (34)$$

$$I_{D5} = I_{C1} = I_{L1} - I_{ld}. \quad (35)$$

The operation principle described before features two types of active state. The rate of fall of the current  $I_{L1}$  differs by a factor of two for these two active states. Also, the inductor  $L_2$  can be rated for lower saturation current as compared to the inductor  $L_1$ . This section described the operation principle of the converter in continuous conduction mode (CCM) when the current of the diode  $D_5$  does not drop to zero.

### III. STEADY STATE ANALYSIS AND DISCUSSIONS

#### A. Steady State Analysis

It is evident from the previous section that current  $I_{L1}$  falls by  $\Delta I_{L12}$  during the first active state:

$$L \frac{\Delta I_{L12}}{D_{A1} \cdot T} = V_{C1} - V_{IN}. \quad (36)$$

Substituting (12) into (36), a ratio between  $D_{A1}$  and  $D_S$  can be found:

$$D_{A1} = D_S \cdot \frac{V_{IN}}{V_{C1} - V_{IN}}. \quad (37)$$

In (37) and before, it can be assumed that  $V_{C1} \geq V_{IN}$ . To find the ratio between  $D_{A2}$  and  $D_S$ , first, the voltage-second balance has to be applied to the inductor  $L_2$ :

$$D_S \cdot V_{C1} = D_{A2} \cdot \frac{V_{C1} - V_{IN}}{2}. \quad (38)$$

Then the required duty cycle ratio from (38) is as follows:

$$D_{A2} = D_S \cdot \frac{2 \cdot V_{C1}}{V_{C1} - V_{IN}}. \quad (39)$$

From (37) and (39) it follows that

$$1 - D_S = D_{A1} + D_{A2} = D_S \cdot \left( \frac{V_{IN} + 2 \cdot V_{C1}}{V_{C1} - V_{IN}} \right). \quad (40)$$

The dc voltage gain  $G$  of the cSL-qSBI follows from (40):

$$G = \frac{V_{C1}}{V_{IN}} = \frac{1}{1 - 3 \cdot D_S}. \quad (41)$$

#### B. Comparison with Counterparts

Comparison of the dc voltage gains of the cSL-qSBI proposed with other IS inverters with extended boost features is shown in Fig. 7. The following counterparts were taken for this comparison: the conventional ZSI and qZSI [1],[5], the diode assisted qZSI (DA-qZSI) [30], the switched-inductor SBI [28], the capacitor assisted qZSI (CA-qZSI) [11], the continuous input current switched-inductor quasi-Z-source inverter (cSL-qZSI) [26], the switched-inductor ZSI (SL-ZSI) [23], the ripple input current switched-inductor quasi-Z-source inverter (rSL-qZSI) [26], and the SL-qSBI [29].

All IS inverters used in the comparison were divided into five groups by the dc voltage gain. The cSL-qSBI proposed belongs to group 4 by the dc voltage gain. It means that it features up to 25% lower dc voltage gain than that of group 5 and up to 30% higher than that of group 3.

It is evident from Fig. 7 that group 5 has the best voltage step-up performance, while all IS inverters in this group have either discontinuous current (SL-ZSI), which is not appropriate for most of emerging applications, or continuous input current with high ripple due to two-step modulation of the input current by the SL (rSL-qZSI and SL-qSBI).

All inverters in group 4 provide continuous input current with low ripple. However, the CA-qZSI and cSL-qZSI have high number of components and thus cannot provide high efficiency or power density. Hence, the cSL-qSBI proposed features both low input current ripple and low number of components. These properties make the cSL-qSBI advantageous over its counterparts for modern power electronics applications, like renewable and alternative energy, battery applications, etc. It can provide high efficiency and power density at low realization cost.

#### C. Continuous and Discontinuous Conduction Modes

The operation principle presented above deals with CCM of the cSL-qSBI when the current of the diode  $D_5$  does not drop to zero during the second active state. Otherwise, the inverter will operate in the discontinuous conduction mode (DCM)

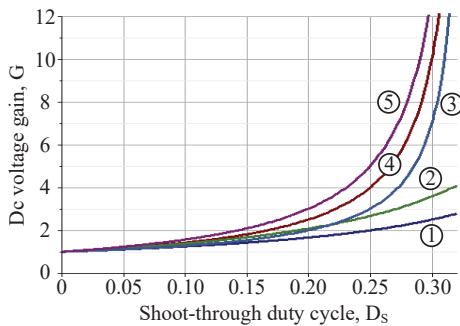


Fig. 7. Comparison of dc voltage gain of IS inverters with extended boost features.

- ① Conventional ZSI or qZSI [1]:  $G = \frac{1}{1 - 2 \cdot D_S}$
- ② DA-qZSI [30]:  $G = \frac{1}{2 \cdot D_S^2 - 3 \cdot D_S + 1}$
- ③ SL-SBI [28]:  $G = \frac{1 - D_S}{1 - 3 \cdot D_S}$
- ④ CA-qZSI [11], cSL-qZSI [26], **cSL-qSBI**:  $G = \frac{1}{1 - 3 \cdot D_S}$
- ⑤ SL-ZSI [23], rSL-qZSI [26], SL-qSBI [29]:  $G = \frac{1 + D_S}{1 - 3 \cdot D_S}$



with excessive output voltage (voltage over-boost). This mode is possible when an IS inverter operates with small inductance in an IS network or supplies a load with low power factor [31]. Undesirable voltage stress of the inverter components can be avoided if an additional switch is connected in parallel with the diode  $D_5$ , as shown in Fig. 8. The switch  $S_b$  can be turned on during the second active state to enable reverse conduction in that branch and thus avoid DCM.

#### IV. SIMULATION RESULTS

Simulation study of the cSL-qSBI was performed to verify theoretical predictions. Simulation model was implemented in PSIM 9 according to the equivalent circuit shown in Fig. 4. The parameters used for the simulation are shown in Table I. Simulation waveforms are shown in Fig. 9. The idealized  $V_{C1}$  voltage was expected at the level of 364 V, while simulation shows 355 V due to losses in semiconductor components. It also shows the corner point of the current  $I_{L1}$ , when its rate of falling changes by factor of two at the instant between states  $A1$  and  $A2$ . The converter provides the dc voltage gain of 1.775 with the shoot-through duty cycle equal to 0.15.

The simulation results presented are in good agreement with the analysis presented in two previous sections. Losses in semiconductor components influence voltage step-up performance slightly. Hence, the cSL-qSBI is a promising solution due its simplicity and consequently high efficiency.

#### V. CONCLUSIONS

This paper proposes a novel improved switched-inductor quasi-switched-boost inverter that features continuous input current with low current ripple. This topology is advantageous over other impedance-source inverters with extended boost features implemented through cascading of components. It has simple structure and high dc voltage gain. The inverter proposed can provide high efficiency and power density. Moreover, it can be easily modified to avoid undesirable DCM operation by adding one more auxiliary switch. The simulation study performed considering losses in semiconductors corroborates theoretical predictions.

Further research could be directed towards modulation techniques and experimental verification of the inverter proposed. Also, operation with small inductance value and low power factor has to be analyzed.

TABLE I  
PARAMETERS USED IN SIMULATION MODEL

Parameter	Value
Switching frequency	25 kHz
$L_1, L_2$	500 $\mu$ H
$C_1$	100 $\mu$ F
$V_{IN}$	200 V
$R_{ld}$	50 $\Omega$
Forward voltage drop of the diodes	1.5 V
Saturation voltage of the switches	2 V
Shoot-through duty cycle, $D_S$	0.15
Input power	2.25 kW

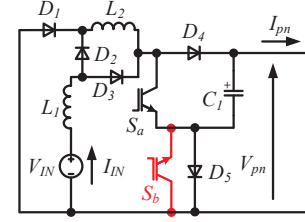


Fig. 8. Modified cSL-qSBI for operation with low inductance or low power factor.

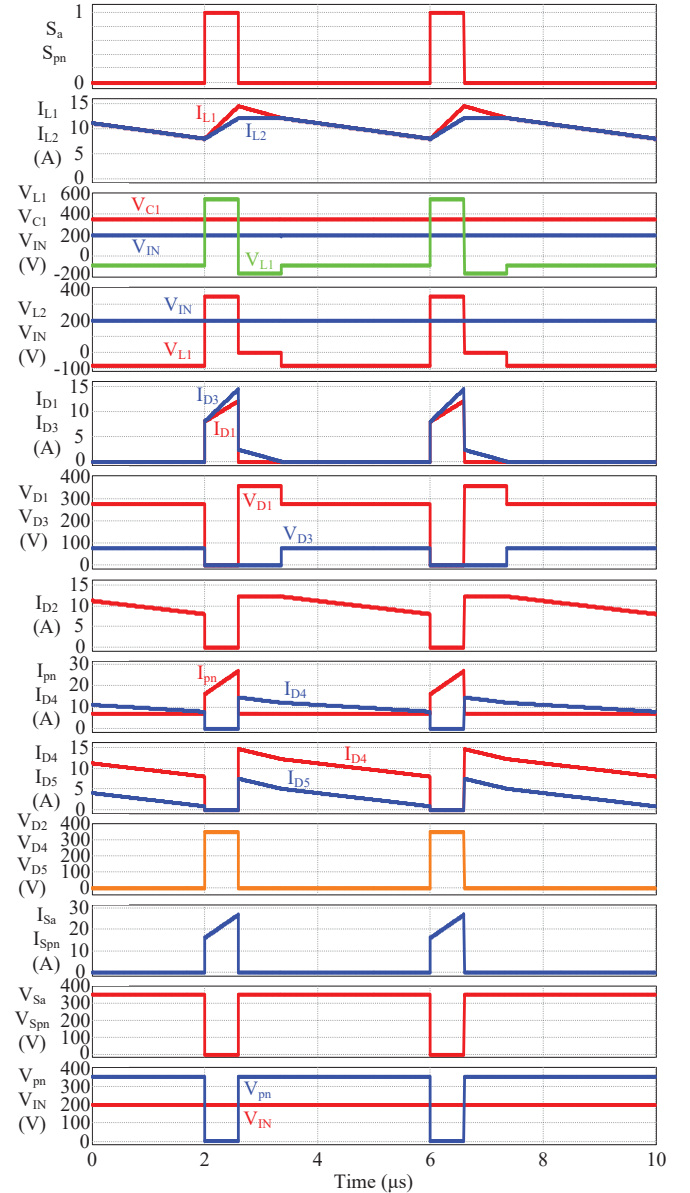


Fig. 9. Simulation results of the cSL-qSBI.

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