TELECOMMUNICATIONS AND ELECTRONICS
ISSN 1407-8880 TELEKOMUNIKĀCIJAS UN ELEKTRONIKA 2008-8880

Investigation of EMI reduction and output voltage ripple minimization using interleaved buck converters

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Abstract – The possibilities of output voltage quality improvement and EMI reduction using interleaved buck converters are studied in this work. The problem of excessive output voltage ripples arises when the spread spectrum method is applied to single buck converter in order to reduce the level of EMI emissions. The investigation shows that it is possible to significantly reduce ripple only at certain values of maximal duty ratios D. At other D values pulsation magnitude is considerably larger, although in comparison with single buck converter it is still smaller. Interleaving of converters also leads to input conducted noise reduction.

Keywords: interleaved buck converters, EMI, spread spectrum.

I. INTRODUCTION

Modern electronic devices in most cases are equipped with switch mode power supplies (SMPS), which have several great advantages over linear ones: smaller weight, size and much higher efficiency. The price of these benefits is higher level of electromagnetic noise emissions – both radiated and conducted. High efficiency is achieved through the impulse (switching) operating regime of SMPS. But it is the cause of electromagnetic interference (EMI) problems. Any impulse device has inherited current and voltage signals with extremely sharp edges, that means there are high di/dt and dv/dt values. Rapid current and voltage transitions may cause high frequency oscillations on parasitic inductances and capacitances of the circuit elements. Also signals with high di/dt or dv/dt have very densit spectral content with considerable harmonic levels at the frequencies in tens and hundreds MHz region. And as operating frequency of SMPS continues to grow, the noise harmonics can reach GHz region, thus becoming a serious threat to wireless communication systems. The regulatory agencies all over the world are placing limits on electromagnetic noise emissions produced by this type of electronic devices, but engineers are forced to investigate new methods of eliminating the EMI level.

Although, the number of topologies existing for SMPS is rather large, the causes of electromagnetic noise are similar in the most of them. And for this reason the EMI reduction methods are almost all the same.

In the recent years many EMI reduction techniques were investigated in details. Here only some of them will be mentioned:

- SMPS printed circuit boards are designed, taking into account some special requirements that allow to eliminate parasitic capacitances, inductances and to compensate EMI;
- RC filters at the clock source are placed to control rise and fall times; slower rise and fall times (as slow as possible for specific device) result in lower emitted harmonic levels; unfortunately, this leads to increase of switching loses, and as a result to lower efficiency of SMPS;
- when the source of the signal noise cannot be eliminated, filtering is recommended as the last resort. EMI filters and ferrite beads are commonly available filters; ferrite beads add inductance to suppress high frequency noise.

One more method to reduce EMI is the spread spectrum method. To clearly understand the main idea of spread spectrum in SMPS it should be mentioned that main parameters (frequency, duty ratio and in some cases magnitude) of any current or voltage signal in SMPS (also input current and output voltage) are determined by the control signal. These signals spectrum contains component at switching frequency (fsw) and its harmonics. Thus noise energy is concentrated in very narrow bands at fsw and its multiples. Modulation of control signal's parameters (frequency, pulse width or pulse position) will result in spreading energy of each harmonic over a wider frequency range. Thus the peak noise levels will be lowered. The main advantage of spread spectrum is that there is no need to add extra components to the circuit – only control circuit should be slightly changed.

Other researchers [1-5] showed that the most appropriate for SMPS is frequency modulation of control signal with constant duty cycle. In the previous research [6], this spread spectrum technique was applied to buck converter, using different types of modulating signals – chaotic, random, sinusoidal. It has been established, that the application of spread spectrum method to single open loop buck converter not only caused attenuation of spectral

harmonics but also led to noticeable increase of the output voltage ripple magnitude, thus worsening output voltage quality. Possibilities of output voltage ripple minimization, using one particular method – interleaving of buck converters - are investigated in this research.

In today's approach, trial-and-error methods often are used to find the proper EMI suppression solution. While this is ultimately successful, it is time-consuming, expensive, and often difficult to combine with optimized performance of the power supply. For receiving results of investigation in the most timesaving way, the EMI characteristics of SMPS are needed to be analyzed as effectively as possible. This makes beneficial the use of different simulation programs in the process of SMPS design. In this study Matlab and Simulink were used to analyze effects of interleaving buck converters. Simulink has build in SimPowerSystems blockset which allows modeling of power circuits, but Matlab have vary powerful signal analysis tools to perform spectral analysis.

II. DEVICE UNDER TEST –INTERLEAVED BUCK CONVERTERS

The fundamental limitation of the single-phase buck converter is the trade-off between efficiency and switching frequency. Output ripple and dynamic response improve with increased switching frequency. The physical size and value of the filter inductor and capacitors become smaller at higher switching frequencies. But there is, however, a practical limitation to the switching frequency: switching losses increase with frequency, and resulting efficiency tends to be lower.

The multi-phase interleaved buck topology offers a solution to the discrepancy meant. The fundamental frequency is effectively multiplied by the number of phases used, improving transient response. Other intrinsic advantages of this solution include reduced input and output capacitor RMS currents; reduced EMI filtering requirements; lower profile and decreased PCB size; better thermal and forced convection performance; improved reliability and power stage redundancy; and easier power train component selection [7].

The schematic of an interleaved buck converter implementation with N phases is shown in Fig. 1.

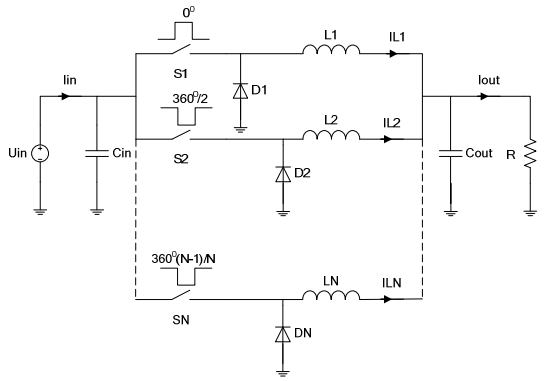

Fig.1. N interleaved buck converters

As it could be seen from the Fig.1 all converters have common input and output capacitors and are feeding common load, but each converter has its own switch, inductor and recovery diode.

Switches are driven at a duty cycle ratio *D*, where:

$$D = T_{on} / T_{sw} = U_{OUT} / U_{IN} \qquad (1)$$

All switches operate at constant switching frequency, $f_{sw}=1/T_{sw}$, where T_{sw} is the switching period. The oscillators are synchronized such that each phase is driven by gate drive signals of the same switching frequency f_{sw} but adjacent phases are phase shifted by 360°/*N*. For example, a three phase converter is driven by signals at 0, 120, and 240 degrees (see Fig.2).The input and output of the each buck converter are paralleled such that the fundamental ripple frequency at the input and output is Nf_{sw}.

The output filter consists of inductive elements L1=L2=...= LN and capacitance C_{out}. C_{in} denotes the input capacitance. Input and output currents are I_{in} and I_{out}, respectively. As it was already mentioned, the filter

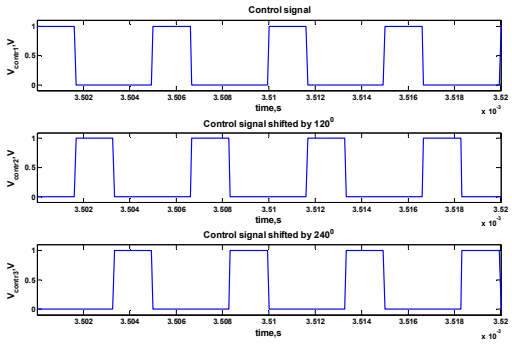

Fig.2. Example of the control signals for three-phase buck converters

inductors are represented as separate elements in each phase whereas the input and output capacitors are shared.

Assuming ideal current sharing due to interleaving, we can write:

$$D_1 = D_2 = ... = D_N = V_{OUT} / V_{IN}$$
$$I_{L1} = I_{L2} = ...I_{LN} = I_{OUT} / N \qquad (2)$$

If the per-phase inductors have equal inductance value and experience equal applied voltage, then the inductor ripple currents are equal. The peak-to-peak single inductor ripple current, ΔI_L, is given by Eq. 3:

$$\Delta I_L = I_{LMAX} - I_{LMIN} = V_{OUT}(1-D)/Lf_s \qquad (3)$$

where I_{LMAX} and I_{LMIN} are the inductor peak and valley currents, respectively.

The output ripple current of the interleaved buck flows into the output capacitor as expressed by Eq. 4, where *m*= *floor*(*N*•*D*) and the floor function returns the greatest integer value less than the argument.

$$I_{C_{OUT}pk-pk} = \frac{Vout}{Lf_s}\left[1-\frac{m}{ND}\right][1+m-ND] \qquad (4)$$

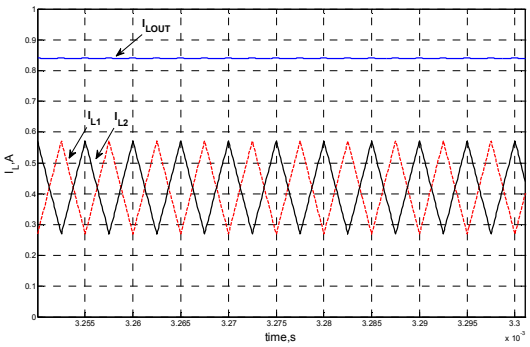

Fig.3. Currents I_{L1}, I_{L2} and total current I_{LOUT}

For example, if $D < 1/N$, $m = 0$ and Eq. 4 simplifies to

$$I_{C_{OUT}pk-pk} = V_{OUT}(1-D)/Lf_s \qquad (5)$$

This term is smaller than the individual inductor ripple current given by Eq. 3 due to current cancellation of the interleaved buck converters (see Fig.3).

As the total current I_{LOUT} feeds the load, the aforementioned current ripple minimization effect allows noticeably reduce the magnitude of output voltage ripple in comparison with the single buck converter [8-10].

III. SIMULATION MODEL AND RESULTS

In order to investigate the mentioned features of interleaved converters, SIMULINK model of interleaved buck converters was designed. As it could be seen from Fig.1, all buck converters under study have common input and output capacitors and feed one common load resistor.

The power plant was created using specialized SimPowerSystems blockset elements. Circuit parameters are summarized in the following table.

Table 1.

Buck converter parameters	
Parameter	**Value**
f_{sw}	20000 kHz
U_{in}	9 V
C_{in}	940 µF
C_{out}	660 µF
L_1,L_2...L_4	39 µH
R_{LOAD}	5 Ω

The PWM control block was designed especially for interleaved buck converters using simple SIMULINK blocks and embedded matlab function block for generating sawtooth time reference signal (see Fig. 4). With this PWM block it is possible to generate control signals for N interleaved converters, changing the frequency and controlling duty ratios. The maximum number of interleaved converters used in simulations was N=4.

This PWM also allows the change of switching frequency at certain time instants accordingly to the signal values of outer source. This function was used to investigate the application of spread spectrum technique to interleaved converters.

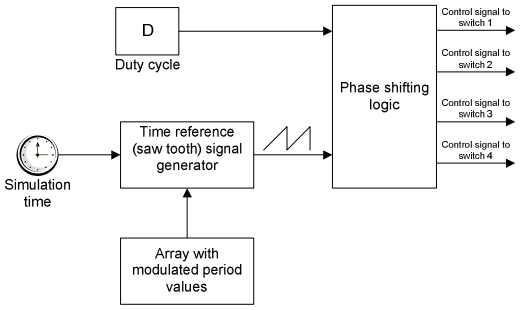

Fig. 4.Block diagram of four interleaved buck converters control with enabled spread spectrum

If the load resistance or input voltage is varied during the operation, to ensure constant output voltage, the duty cycle of the control signal should be accordingly changed, as a result other circuit descriptive parameters are altered. Within the research the dependence of input current harmonics and output voltage ripple magnitudes of two interleaved buck converters on the value of control signal duty cycle is examined. The duty cycle is varied from 5% to 50% and the first 5 harmonics of input current are examined. Results are shown in the Fig.5. and Fig.6. It can be seen that with the decrease of D and respectively power consumption from source, harmonic level also becomes lower.

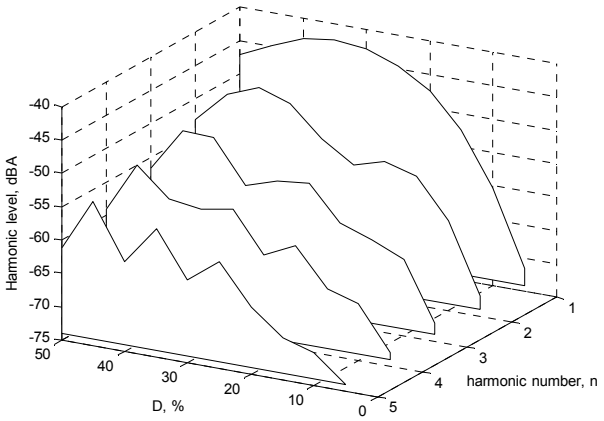

Fig. 5.Input current spectrum

To examine the dependence of output voltage ripples on the number of interleaved converters, ripple magnitudes were evaluated for single buck and N=2,3,4 interleaved converters. As changing the duty cycle, the DC component of output voltage varies, then to evaluate output voltage quality, relative values of output voltage ripple magnitudes are used (representing the ratio of output voltage ripple magnitude to output voltage DC component). As it could be seen from Fig.7 we can observe the reduction of output voltage ripple magnitude with the increase of number of interleaved buck converters.

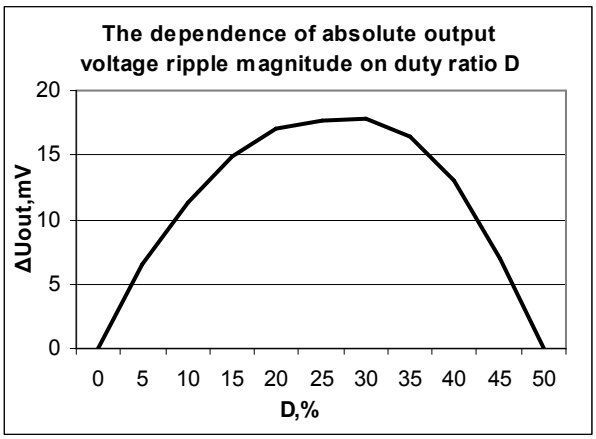

Fig.6.The dependence of output voltage ripple peak-to-peak magnitude on duty ratio D for 2 interleaved buck converters

To evaluate how the application of spread spectrum technique influences interleaved converter's input current spectrum and output voltage ripple magnitude, two modulating signals were observed: sinusoidal with f_{mod}=5kHz and the random signal with uniform distribution. The maximal frequency deviation in both cases was 10%. For two interleaved converters with D=0.5 output voltage ripple for both modulating signals does not exceed 1mV.

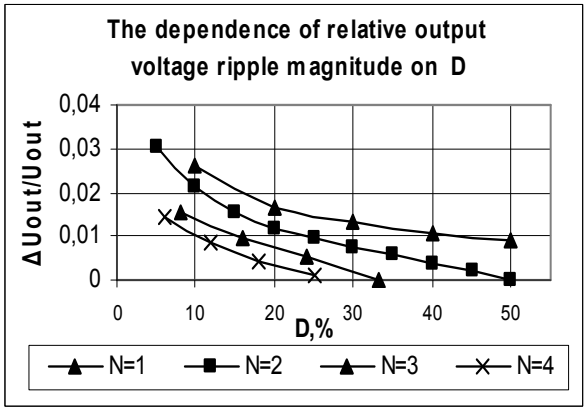

Fig.7. The dependence of relative output voltage ripple magnitude on duty ratio D for N interleaved buck converters

When D=0.25, also for two mentioned modulating signals amplitudes of pulsations were approximately identical and equal to 20mV. For comparison: the nonmodulated single buck converter's output voltage ripple is equal to 36 mV (D=0.5). Analysis of input current spectra revealed the same effects that were discussed in [6].

IV. CONCLUSIONS

During the investigation it has been ascertained that the interleaving of buck converters leads to substantial ripple cancellation only in the cases when duty ratios for each switch were: $D=T_{sw}/N$, where T_{sw} is nominal switching period and N is number of interleaved converters. It is so because in this case each inductor current is shifted in phase and the resulting output current, which is the sum of inductor currents of all N stages, is equal to mean output current with negligible ripple. If $D=T_{sw}/2N$, then the current compensation is not so effective and output voltage ripple is maximal. But anyway it is smaller then in case of single buck.

One more consideration should be taken into account: maximum output voltage in the case of interleaved converters is $U_{out}=D_{max}U_{in}$, where D_{max} is T_{sw}/N. If D is larger then D_{max} currents in inductors are not equal, that in turn leads to overheating of one of transistors. For this reason interleaving of converters may not be appropriate technique when input voltage is not high enough to ensure nominal output voltage at $D<D_{max}$.

Because of higher output voltage quality and lower peak EMI emissions it's advantageous to use interleaved buck converters together with spread spectrum method.

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